Advanced Information
Preliminary Datasheet

OV7725 Color CMOS VGA (640x480) CAMERACHIP™ Sensor with OmniPixel2™ Technology

General Description

The OV7725 CAMERACHIP™ image sensor is a low voltage CMOS device that provides the full functionality of a single-chip VGA camera and image processor in a small footprint package. The OV7725 provides full-frame, sub-sampled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This device has an image array capable of operating at up to 60 frames per second (fps) in VGA with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, OmniVision sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, blooming, etc., to produce a clean, fully stable color image.

Note: The OV7725 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Standard SCCB interface
- Output support for Raw RGB, RGB (GRB 4:2:2, RGB565/555/444) and YCbCr (4:2:2) formats
- Supports image sizes: VGA, QVGA, and any size scaling down from CIF to 40x30
- VarioPixel® method for sub-sampling
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), and anti-blooming
- ISP includes noise reduction and defect correction
- Lens shading correction
- Saturation level auto adjust (UV adjust)
- Edge enhancement level auto adjust
- De-noise level auto adjust
- Frame synchronization capability

Ordering Information

Product	Package
OV07725-VL1A (Color, lead-free)	28-pin CSP2

Applications

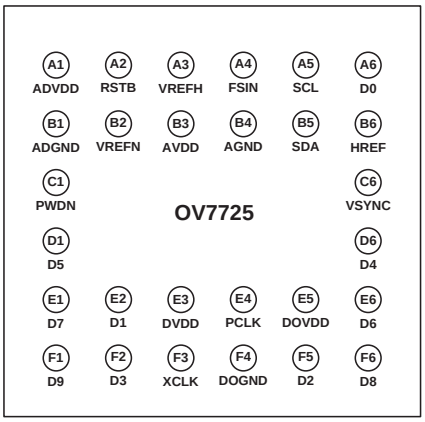
- Cellular and picture phones
- Toys
- PC Multimedia
- Digital still cameras

Key Specifications

Array Size		640 x 480
Power Supply	**Digital Core**	1.8VDC ± 10%
	Analog	3.0V to 3.3V
	I/O[a]	1.7V to 3.3V
Power Requirements	**Active**	120 mW typical (60 fps VGA, YUV)
	Standby	< 20 µA
Temperature Range		-20°C to +70°C
Output Format (8-bit)		• YUV/YCbCr 4:2:2 • RGB565/555/444 • GRB 4:2:2 • Raw RGB Data
Lens Size		1/4"
Lens Chief Ray Angle		25° non linear
Max Image Transfer Rate		60 fps for VGA
Sensitivity		TBD
S/N Ratio		TBD
Dynamic Range		TBD
Scan Mode		Progressive
Electronic Exposure		Up to 510:1 (for selected fps)
Pixel Size		6.0 µm x 6.0 µm
Dark Current		TBD
Well Capacity		TBD
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		3984 µm x 2952 µm
Package Dimensions		5345 µm x 5265 µm

a. I/O power should be 2.45V or higher when using the internal regulator for Core (1.8V); otherwise, it is necessary to provide an external 1.8V for the Core power supply

Figure 1 OV7725 Pinout (Top View)



Version 1.0, September 12, 2006

Functional Description

Figure 2 shows the functional block diagram of the OV7725 image sensor. The OV7725 includes:

- Image Sensor Array (total array of 656 x 488 pixels, with active pixels 640 x 480 in YUV mode)
- Analog Signal Processor
- A/D Converters
- Test Pattern Generator
- Digital Signal Processor (DSP)
- Image Scaler
- Timing Generator
- Digital Video Port
- SCCB Interface

Figure 2 Functional Block Diagram

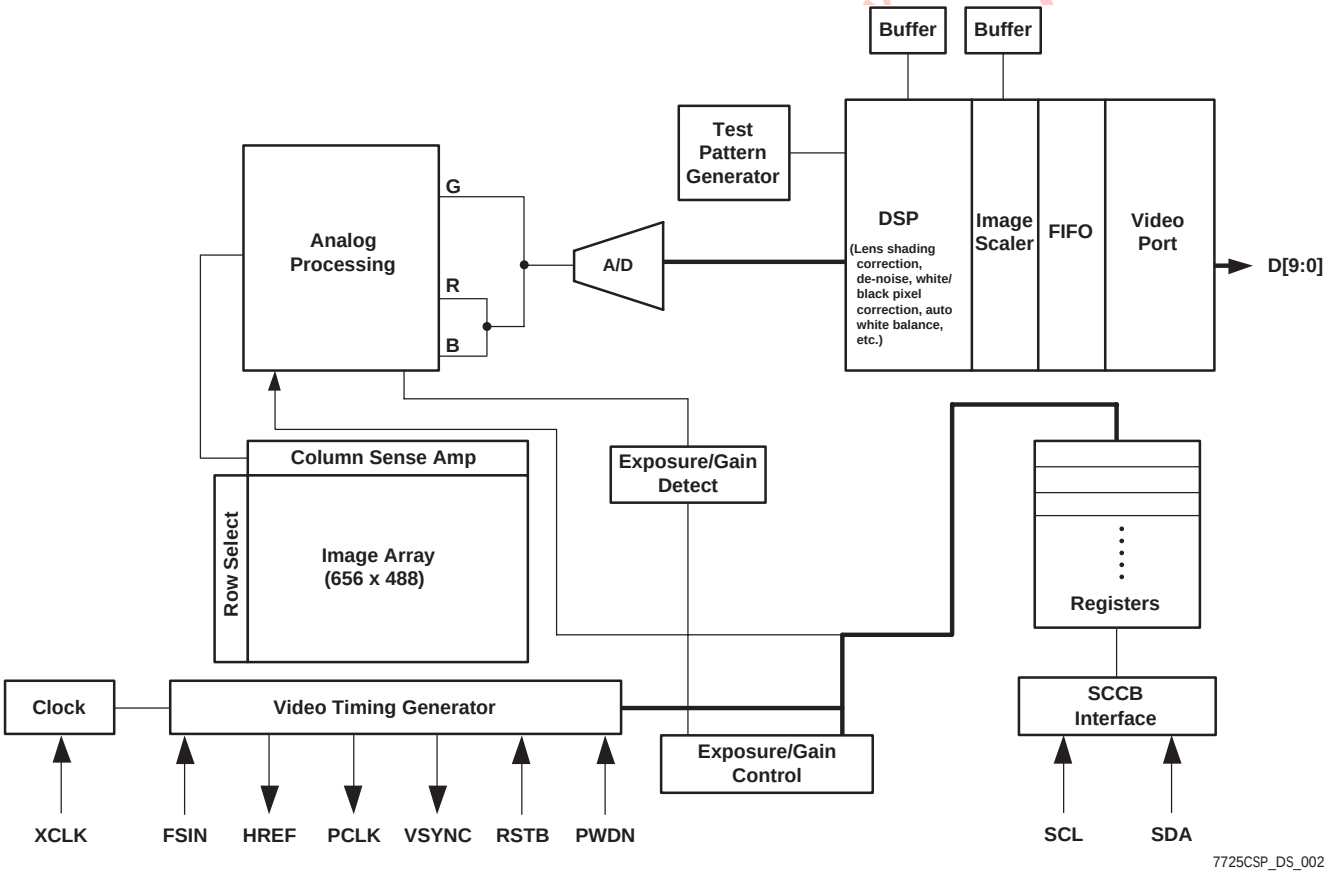
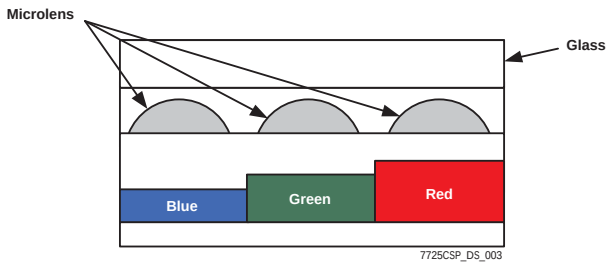


Image Sensor Array

The OV7725 sensor has an image array of 656 x 488 pixels for a total of 320,128 pixels, of which 640 x 480 pixels are active (307,200 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to a 10-bit analog-to-digital (A/D) converter shared by G and BR channels. This A/D converter operates at speeds up to 12 MHz and is fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Test Pattern Generator

The Test Pattern Generator features the following:

- 8-bar color bar pattern
- Shift "1" in output pin

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit

Image Scaler

This block controls all output and data formatting required prior to sending the image out. This block scales YUV/RGB output from VGA to CIF and almost any size under CIF.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP sensor operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Function/Description
A1	ADVDD	Power	ADC power supply
A2	RSTB	Input	System reset input, active low
A3	VREFH	Reference	Reference voltage - connect to ground using a 0.1 µF capacitor
A4	FSIN	Input	Frame synchronize input
A5	SCL	Input	SCCB serial interface clock input
A6	D0[a]	Output	Data output bit[0]
B1	ADGND	Power	ADC ground
B2	VREFN	Reference	Reference voltage - connect to ground using a 0.1 µF capacitor
B3	AVDD	Power	Analog power supply
B4	AGND	Power	Analog ground
B5	SDA	I/O	SCCB serial interface data I/O
B6	HREF	Output	HREF output
C1	PWDN	Input (0)[b]	Power Down Mode Selection 0: Normal mode 1: Power down mode
C6	VSYNC	Output	Vertical sync output
D1	D5	Output	Data output bit[5]
D6	D4	Output	Data output bit[4]
E1	D7	Output	Data output bit[7]
E2	D1	Output	Data output bit[1]
E3	DVDD	Power	Power supply (+1.8 VDC) for digital logic core
E4	PCLK	Output	Pixel clock output
E5	DOVDD	Power	Digital power supply for I/O (1.7V ~ 3.3V)
E6	D6	Output	Data output bit[6]
F1	D9[c]	Output	Data output bit[9]
F2	D3	Output	Data output bit[3]
F3	XCLK	Input	System clock input
F4	DOGND	Power	Digital ground
F5	D2	Output	Data output bit[2]
F6	D8	Output	Data output bit[8]

a. D[9:0] for 10-bit Raw RGB data (D[9] MSB, D[0] LSB)

b. Input (0) represents an internal pull-down resistor.

c. D[9:2] for 8-bit YUV or RGB565/RGB555 (D[9] MSB, D[2] LSB)

Electrical Characteristics

Table 2 Operating Conditions

Parameter	Min	Max
Operating temperature	-20°C	+70°C
Storage temperature[a]	-40°C	+125°C

a. Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.

Table 3 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-C}	3 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+0.5V
Lead-free Temperature, Surface-mount process		245ºC

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 4 DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	–	3.0	3.3	3.6	V
V_{DD-C}	DC supply voltage – Digital Core	–	1.62	1.8	1.98	V
V_{DD-IO}	DC supply voltage – I/O power	–	2.5	–	3.3	V
I_{DDA}	Active (Operating) Current	See Note [a]		10 + 8[b]		mA
$I_{DDS-SCCB}$	Standby Current	See Note [c]		1		mA
$I_{DDS-PWDN}$	Standby Current			10	20	µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [d]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = 3.3V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.3V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 30 fps YUV output, no I/O loading

b. I_{DD-C} = 10mA, I_{DD-A} = 8mA, without loading

c. V_{DD-A} = 3.3V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.3V
$I_{DDS-SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to a PWDN pin-initiated Standby

d. Standard Output Loading = 25pF, 1.2KΩ

Table 5 Functional and AC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			30	dB
	Red/Blue Adjustment Range			12	dB
Inputs (PWDN, CLK, RESET#)					
f_{CLK}	Input Clock Frequency	10	24	48	MHz
t_{CLK}	Input Clock Period	21	42	100	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f_{SCL}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SCL low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[9:0] (see Figure 5, Figure 6, Figure 7, and Figure 8)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	D[9:0] Setup time	15			ns
t_{HD}	D[9:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-C} = 1.8V, V_{DD-A} = 3.3V, V_{DD-IO} = 3.3V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3.3V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

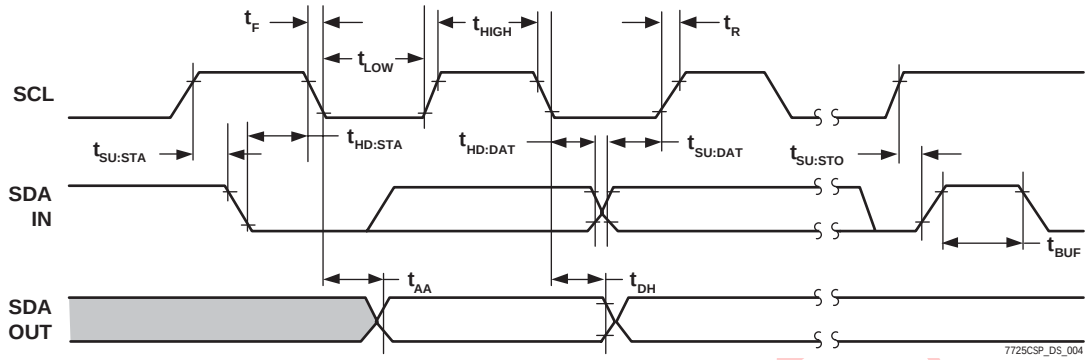


Figure 5 Horizontal Timing

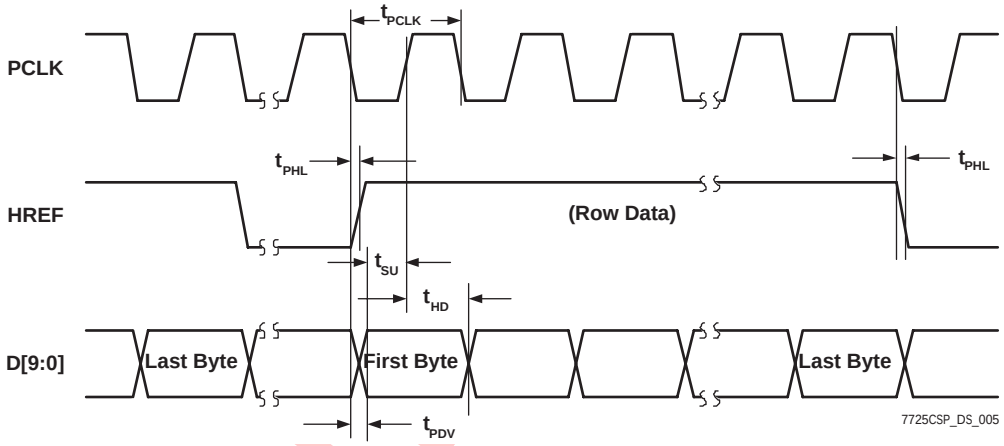
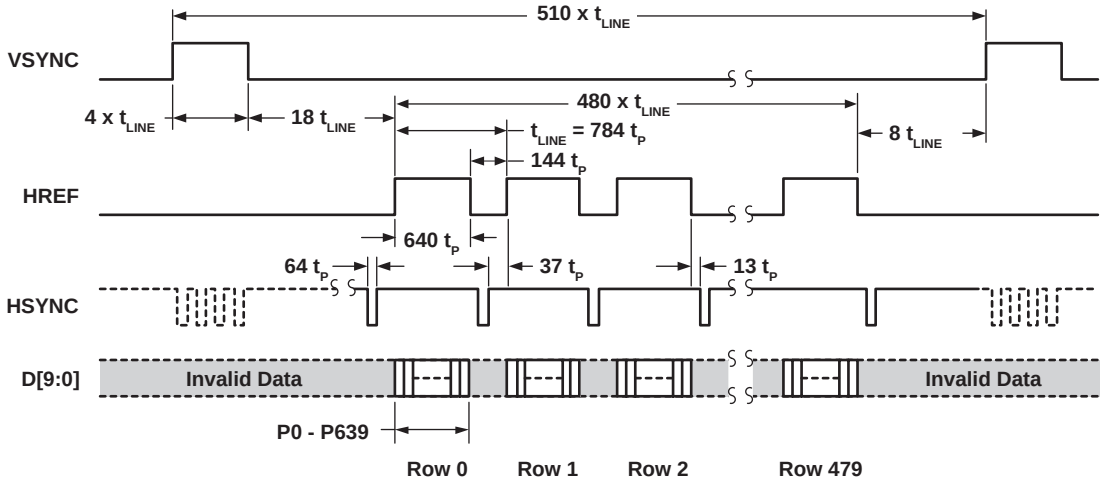


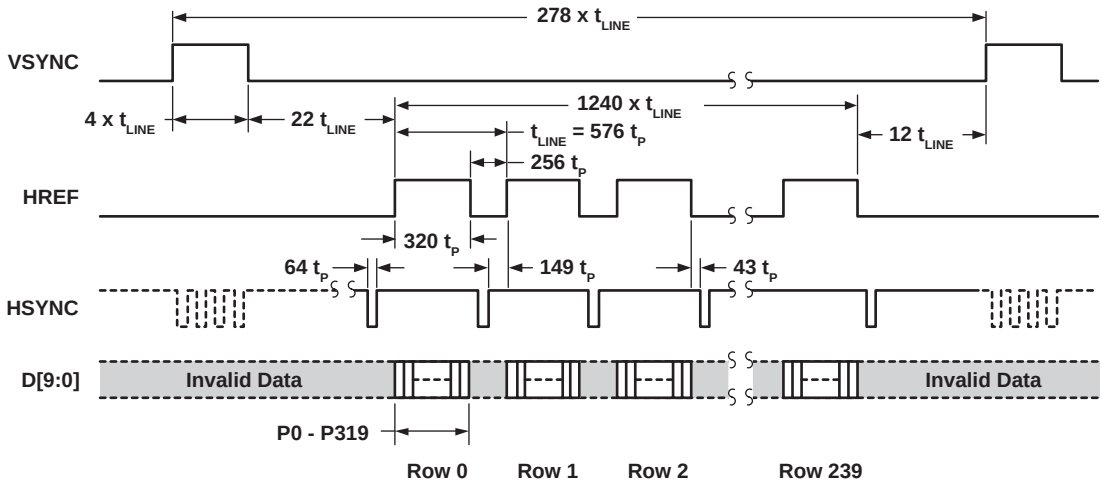
Figure 6 VGA Frame Timing



NOTE:
For Raw data, $t_P = t_{PCLK}$

For YUV/RGB, $t_P = 2 \times t_{PCLK}$

Figure 7 QVGA Frame Timing



NOTE:
For Raw data, $t_P = t_{PCLK}$

For YUV/RGB, $t_P = 2 \times t_{PCLK}$

7725CSP_DS_007

Figure 8 CIF Frame Timing

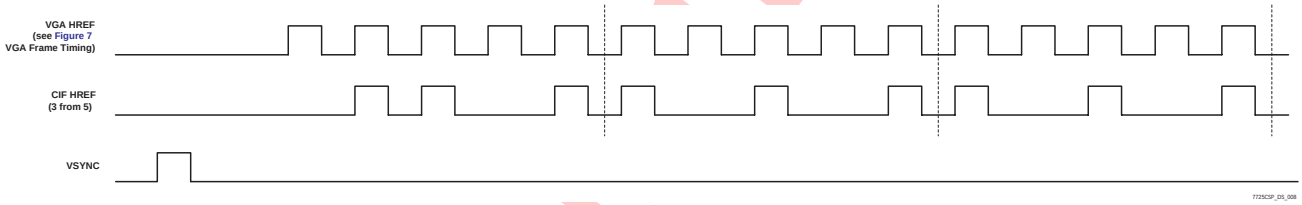


Figure 9 RGB 565 Output Timing Diagram

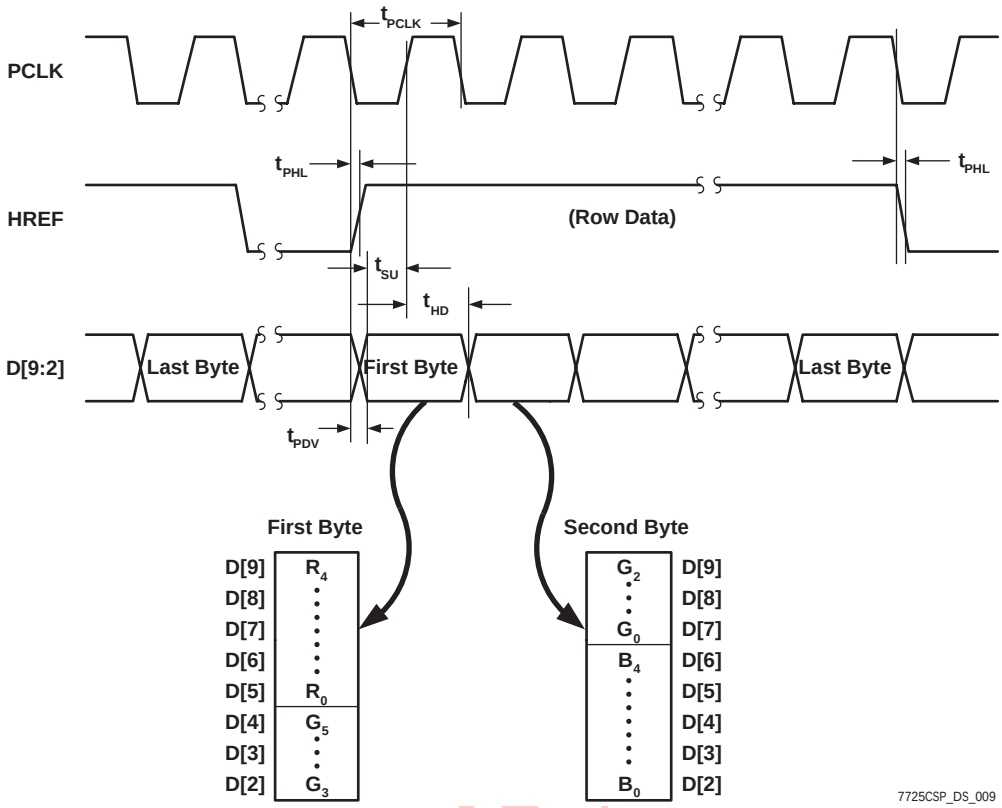


Figure 10 RGB 555 Output Timing Diagram

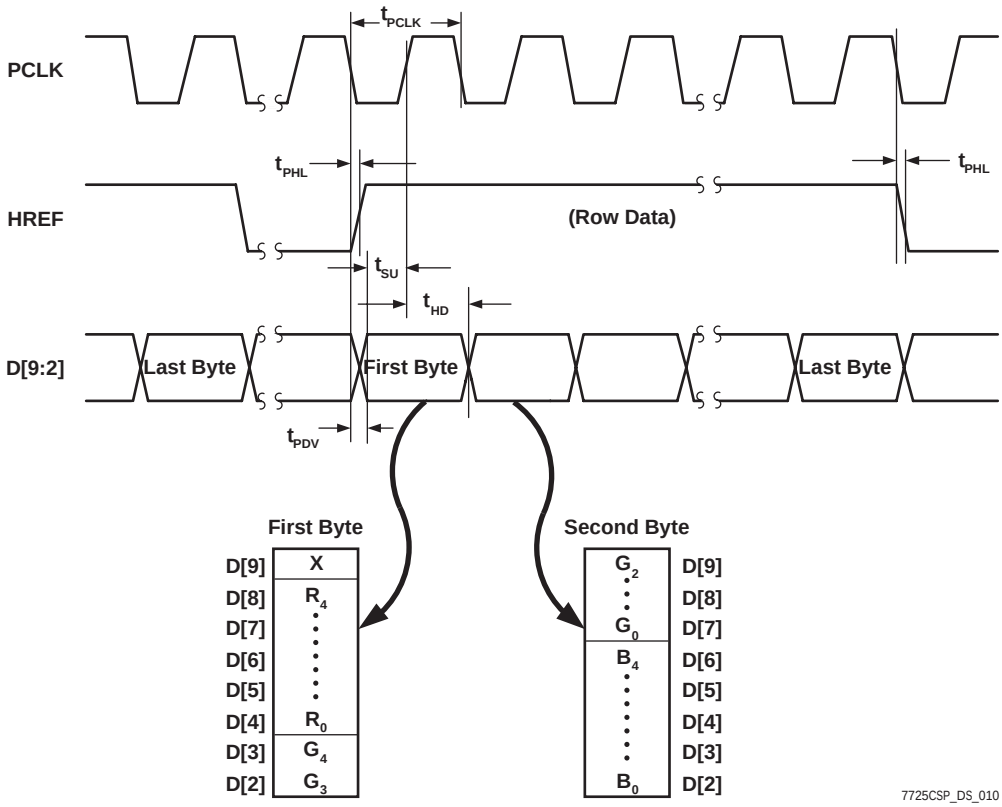
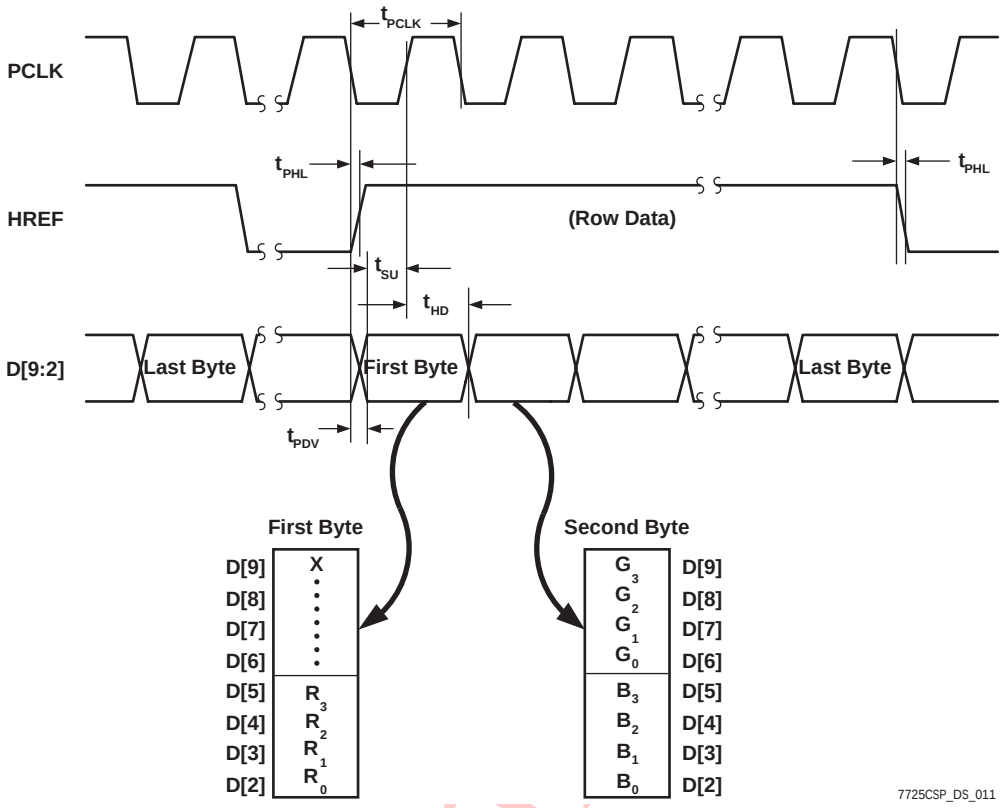


Figure 11 RGB 444 Output Timing Diagram



Register Set

Table 6 provides a list and description of the Device Control registers contained in the OV7725. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 42 for write and 43 for read.

Table 6 Device Control Register List (Sheet 1 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting Bit[7:0]: AGC[7:0] (see GREEN[7:6] (0x03) for AGC[9:8]) • Range: [00] to [FF]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF]
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF]
03	GREEN	00	RW	AWB – Green channel gain setting • Range: [00] to [FF]
04	COM1	00	RW	Common Control 1 Bit[7:2]: Reserved Bit[1:0]: AGC 2 MSBs, AGC[9:8]
05	BAVG	00	RW	U/B Average Level Automatically updated based on chip output format
06	GAVG	00	RW	Y/Gb Average Level Automatically updated based on chip output format
07	RAVG	00	RW	V/R Average Level Automatically updated based on chip output format
08	AECH	00	RW	Exposure Value – AEC MSBs Bit[7:5]: AEC[15:8] (see register AEC for AEC[7:0]} Automatically updated based on chip output format
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Soft sleep mode Bit[3:2]: Pixel clock output delay control • Range: [00] to [11] Bit[1:0]: Output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
0A	PID	77	R	Product ID Number MSB (Read only)
0B	VER	21	R	Product ID Number LSB (Read only)

Table 6 Device Control Register List (Sheet 2 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	COM3	10	RW	Common Control 3 Bit[7]: Vertical flip image ON/OFF selection Bit[6]: Horizontal mirror image ON/OFF selection Bit[5]: Swap B/R output sequence in RGB output mode Bit[4]: Swap Y/UV output sequence in YUV output mode Bit[3]: Swap output MSB/LSB Bit[2]: Tri-state option for output clock at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[1]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[0]: Sensor color bar test pattern output enable
0D	COM4	41	RW	Common Control 4 Bit[7:6]: PLL frequency control 00: Bypass PLL 01: PLL 4x 10: PLL 6x 11: PLL 8x Bit[5:4]: AEC evaluate window 00: Full window 01: 1/2 window 10: 1/4 window 11: Low 2/3 window Bit[3:0]: Reserved
0E	COM5	01	RW	Common Control 5 Bit[7]: Auto frame rate control ON/OFF selection Bit[6]: Auto frame rate control speed selection Bit[5:4]: Auto frame rate max rate control 00: No reduction of frame rate 01: Max reduction to 1/2 frame rate 10: Max reduction to 1/4 frame rate 11: Max reduction to 1/8 frame rate Bit[3:2]: Auto frame rate active point control 00: Add frame when AGC reaches 2x gain 01: Add frame when AGC reaches 4x gain 10: Add frame when AGC reaches 8x gain 11: Add frame when AGC reaches 16x gain Bit[1]: Reserved Bit[0]: AEC max step control 0: AEC increase step has limit 1: No limit to AEC increase step
0F	COM6	43	RW	Common Control 6 Bit[7:1]: Reserved Bit[0]: Auto window setting ON/OFF selection when format changes

Table 6 Device Control Register List (Sheet 3 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
10	AEC	40	RW	Exposure Value Bit[7:0]: AEC[7:0] (see register AECH for AEC[15:8])
11	CLKRC	80	RW	Internal Clock Bit[7]: Reserved Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(input clock)/(Bit[5:0]+1) • Range: [0 0000] to [1 1111]
12	COM7	00	RW	Common Control 7 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Resolution selection 0: VGA 1: QVGA Bit[5]: ITU656 protocol ON/OFF selection Bit[4]: Reserved Bit[3:2]: RGB output format control 00: GBR4:2:2 01: RGB565 10: RGB555 11: RGB444 Bit[1:0]: Output format control 00: YUV 01: Processed Bayer RAW 10: RGB 11: Bayer RAW
13	COM8	8F	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit 0: Step size is limited to vertical blank 1: Unlimited step size Bit[5]: Banding filter ON/OFF Bit[4]: Enable AEC below banding value Bit[3]: Fine AEC ON/OFF control Bit[2]: AGC Enable Bit[1]: AWB Enable Bit[0]: AEC Enable

Table 6 Device Control Register List (Sheet 4 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COM9	4A	RW	Common Control 9 Bit[7]: Histogram or average based AEC/AGC selection Bit[6:4]: Automatic Gain Ceiling - maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101 64x 110: 128x 111: Not allowed Bit[3]: Reserved Bit[2]: Drop VSYNC output of corrupt frame Bit[1]: Drop HREF output of corrupt frame Bit[0]: Reserved
15	COM10	00	RW	Common Control 10 Bit[7]: Output negative data Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 0: Free running PCLK 1: PCLK does not toggle during horizontal blank Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: VSYNC option 0: VSYNC changes on falling edge of PCLK 1: VSYNC changes on rising edge of PCLK Bit[1]: VSYNC negative Bit[0]: Output data range selection 0: Full range 1: Data from [10] to [F0] (8 MSBs)
16	RSVD	XX	–	Reserved
17	HSTART	23 (VGA) 3F (QVGA)	RW	Horizontal Sensor Size
18	HSIZE	A0 (VGA) 50 (QVGA)	RW	Horizontal Frame (HREF column) end high 8-bit (low 2 bits are at HREF[1:0])
19	VSTRT	07 (VGA) 03 (QVGA)	RW	Vertical Frame (row) start high 8-bit (low 1 bit is at HREF[6])
1A	VSIZE	F0 (VGA) 78 (QVGA)	RW	Vertical Sensor Size
1B	PSHFT	40	RW	Data Format - Pixel Delay Select (delays timing of the D[9:0] data relative to HREF in pixel units) • Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	RSVD	XX	–	Reserved

Table 6 Device Control Register List (Sheet 5 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1F	LAEC	00	RW	Fine AEC Value - defines exposure value less than one line period
20	COM11	10	RW	Common Control 11 Bit[7:2]: Reserved Bit[1]: Single frame ON/OFF selection Bit[0]: Single frame transfer trigger
21	RSVD	XX	–	Reserved
22	BDBase	FF	RW	Banding Filter Minimum AEC Value
23	DBStep	01	RW	Banding Filter Maximum Step
24	AEW	75	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	63	RW	AGC/AEC - Stable Operating Region (Lower Limit)
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: High nibble of upper limit of fast mode control zone Bit[3:0]: High nibble of lower limit of fast mode control zone
27	RSVD	XX	–	Reserved
28	REG28	??	RW	Register 28 Bit[7:2]: Reserved Bit[1]: Frame sync option (in external frame sync mode, set this bit to 1) Bit[0]: Auto frame adjust option 0: Always decrease frame rate by 2 1: Decrease frame rate by inserting dummy vertical sync equal to maximum exposure lines
29	HOutSize	A0 (VGA) 50 (QVGA)	RW	Horizontal Data Output Size MSBs (2 LSBs at register EXHCH[1:0])
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7:4]: 4 MSB for dummy pixel insert in horizontal direction Bit[3]: Reserved Bit[2]: Vertical data output size LSB Bit[1:0]: Horizontal data output size 2 LSBs
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2C	VOutSize	F0 (VGA) 78 (QVGA)	RW	Vertical Data Output Size MSBs (LSB at register EXHCH[2])
2D	ADVFL	00	RW	LSB of Insert Dummy Lines in Vertical Direction (1 bit equals 1 line)
2E	ADVFH	00	RW	MSB of Insert Dummy Lines in Vertical Direction
2F	YAVE	00	RW	Y/G Channel Average Value
30	LumHTh	80	RW	Histogram AEC/AGC Luminance High Level Threshold
31	LumLTh	60	RW	Histogram AEC/AGC Luminance Low Level Threshold

Table 6 Device Control Register List (Sheet 6 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
32	HREF	00	RW	Image Start and Size Control Bit[7]: Mirror image edge alignment Bit[6]: Vertical HREF window start control LSB Bit[5:4]: Horizontal HREF window start control LSBs Bit[3]: Data output bit shift test pattern ON/OFF control Bit[2]: Vertical sensor size LSB Bit[1:0]: Horizontal sensor size 2 LSBs
33	DM_LNL	00	RW	Dummy Line Low 8 Bits
34	DM_LNH	00	RW	Dummy Line High 8 Bits
35	ADoff_B	80	RW	AD Offset Compensation Value for B Channel
36	ADoff_R	80	RW	AD Offset Compensation Value for R Channel
37	ADoff_Gb	80	RW	AD Offset Compensation Value for Gb Channel
38	ADoff_Gr	80	RW	AD Offset Compensation Value for Gr Channel
39	Off_B	80	RW	Analog Process B Channel Offset Compensation Value
3A	Off_R	80	RW	Analog Process R Channel Offset Compensation Value
3B	Off_Gb	80	RW	Analog Process Gb Channel Offset Compensation Value
3C	Off_Gr	80	RW	Analog Process Gr Channel Offset Compensation Value
3D	COM12	80	RW	Common Control 12 Bit[7:6]: Reserved Bit[5:0]: DC offset compensation for analog process
3E	COM13	E2	RW	Common Control 13 Bit[7]: Analog processing channel BLC ON/OFF control Bit[6]: ADC channel BLC ON/OFF control Bit[5:0]: Reserved
3F	COM14	1F	RW	Edge Enhancement Adjustment Bit[7:4]: Reserved Bit[3:2]: AD offset compensation option x0: Use R/Gr channel value for B/Gb 01: Use B/Gb channel value for R/Gr 11: Use B/Gb/R/Gr channel value independently Bit[1:0]: Analog processing offset compensation option x0: Use R/Gr channel value for B/Gb 01: Use B/Gb channel value for R/Gr 11: Use B/Gb/R/Gr channel value independently
40	COM15	C0	RW	Common Control 15 Bit[7:4]: Reserved Bit[3]: AD add 128 bit offset Bit[2:0]: Reserved
41	COM16	08	RW	Common Control 16 Bit[7:2]: Reserved Bit[1:0]: BLC target 2 LSBs
42	TGT_B	80	RW	BLC Blue Channel Target Value

Table 6 Device Control Register List (Sheet 7 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
43	TGT_R	80	RW	BLC Red Channel Target Value
44	TGT_Gb	80	RW	BLC Gb Channel Target Value
45	TGT_Gr	80	RW	BLC Gr Channel Target Value
46	LCC0	00	RW	Lens Correction Control 0 Bit[7:3]: Reserved Bit[2]: Lens correction control select 0: R, G, and B channel compensation coefficient is set by registers LCC3 (0x49) 1: R, G, and B channel compensation coefficient is set by registers LCC5 (0x4B), LCC3 (0x49), and LCC6 (0x4C), respectively Bit[1]: Reserved Bit[0]: Lens correction enable 0: Disable 1: Enable
47	LCC1	00	RW	Lens Correction Option 1 – X Coordinate of Lens Correction Center Relative to Array Center
48	LCC2	00	RW	Lens Correction Option 2 – Y Coordinate of Lens Correction Center Relative to Array Center
49	LCC3	50	–	Lens Correction Option 3 G channel compensation coefficient when LCC0[2] (0x46) is 1 R, G, and B channel compensation coefficient when LCC0[2] is 0
4A	LCC4	30	–	Lens Correction Option 4 – radius of the circular section where no compensation applies
4B	LCC5	50	RW	Lens Correction Option 5 (effective only when LCC0[2] is high)
4C	LCC6	50	RW	Lens Correction Option 6 (effective only when LCC0[2] is high)
4D	FixGain	00	RW	Analog Fix Gain Amplifier Bit[7:6]: Gb channel fixed gain Bit[5:4]: Gr channel fixed gain Bit[3:2]: B channel fixed gain Bit[1:0]: R channel fixed gain
4E	AREF0	EF	RW	Sensor Reference Control • Range: [00] to [FF]
4F	AREF1	10	RW	Sensor Reference Current Control Bit[7:4]: Sensor reference current control Bit[3]: Internal regulator ON/OFF selection Bit[2]: Reserved Bit[1:0]: Analog reference control
50	AREF2	60	RW	Analog Reference Control • Range: [00] to [FF]
51	AREF3	00	RW	ADC Reference Control • Range: [00] to [FF]
52	AREF4	00	RW	ADC Reference Control • Range: [00] to [FF]

Table 6 Device Control Register List (Sheet 8 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
53	AREF5	24	RW	ADC Reference Control • Range: [00] to [FF]
54	AREF6	7A	RW	Analog Reference Control • Range: [00] to [FF]
55	AREF7	FC	RW	Analog Reference Control • Range: [00] to [FF]
56-5F	RSVD	XX	–	Reserved
60	UFix	80	RW	U Channel Fixed Value Output
61	VFix	80	RW	V Channel Fixed Value Output
62	AWBb_blk	FF	RW	AWB Option for Advanced AWB
63	AWB_Ctrl0	F0	RW	AWB Control Byte 0 Bit[7]: AWB gain enable Bit[6]: AWB calculate enable Bit[5]: Reserved Bit[4:0]: WBC threshold 2
64	DSP_Ctrl1	1F	RW	DSP Control Byte 1 Bit[7]: FIFO enable/disable selection Bit[6]: UV adjust function ON/OFF selection Bit[5]: YUV444 to 422 UV channel option selection Bit[4]: Color matrix ON/OFF selection Bit[3]: Interpolation ON/OFF selection Bit[2]: Gamma function ON/OFF selection Bit[1]: Black defect auto correction ON/OFF Bit[0]: White defect auto correction ON/OFF
65	DSP_Ctrl2	00	RW	DSP Control Byte 2 Bit[7:4]: Reserved Bit[3:0]: Scaling control
66	DSP_Ctrl3	10	RW	DSP Control Byte 3 Bit[7]: UV output sequence option Bit[6]: Reserved Bit[5]: DSP color bar ON/OFF selection Bit[4]: Reserved Bit[3]: FIFO power down ON/OFF selection Bit[2]: Scaling module power down control 1 Bit[1]: Scaling module power down control 2 Bit[0]: Interpolation module power down control
67	DSP_Ctrl4	00	RW	DSP Control Byte 4
68	AWB_bias	00	RW	AWB BLC Level Clip
69	AWBCtrl1	5C	RW	AWB Control 1
6A	AWBCtrl2	11	RW	AWB Control 2
6B	AWBCtrl3	A2	RW	AWB Control 3
6C	AWBCtrl4	01	RW	AWB Control 4

Table 6 Device Control Register List (Sheet 9 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
6D	AWBCtrl5	50	RW	AWB Control 5
6E	AWBCtrl6	80	RW	AWB Control 6
6F	AWBCtrl7	80	RW	AWB Control 7
70	AWBCtrl8	0F	RW	AWB Control 8
71	AWBCtrl9	00	RW	AWB Control 9
72	AWBCtrl10	00	RW	AWB Control 10
73	AWBCtrl11	0F	RW	AWB Control 11
74	AWBCtrl12	0F	RW	AWB Control 12
75	AWBCtrl13	FF	RW	AWB Control 13
76	AWBCtrl14	FF	RW	AWB Control 14
77	AWBCtrl15	FF	RW	AWB Control 15
78	AWBCtrl16	10	RW	AWB Control 16
79	AWBCtrl17	70	RW	AWB Control 17
7A	AWBCtrl18	70	RW	AWB Control 18
7B	AWBCtrl19	F0	RW	AWB Control 19
7C	AWBCtrl20	F0	RW	AWB Control 20
7D	AWBCtrl21	F0	RW	AWB Control 21
7E	GAM1	0E	RW	Gamma Curve 1st Segment Input End Point 0x04 Output Value
7F	GAM2	1A	RW	Gamma Curve 2nd Segment Input End Point 0x08 Output Value
80	GAM3	31	RW	Gamma Curve 3rd Segment Input End Point 0x10 Output Value
81	GAM4	5A	RW	Gamma Curve 4th Segment Input End Point 0x20 Output Value
82	GAM5	69	RW	Gamma Curve 5th Segment Input End Point 0x28 Output Value
83	GAM6	75	RW	Gamma Curve 6th Segment Input End Point 0x30 Output Value
84	GAM7	7E	RW	Gamma Curve 7th Segment Input End Point 0x38 Output Value
85	GAM8	88	RW	Gamma Curve 8th Segment Input End Point 0x40 Output Value
86	GAM9	8F	RW	Gamma Curve 9th Segment Input End Point 0x48 Output Value
87	GAM10	96	RW	Gamma Curve 10th Segment Input End Point 0x50 Output Value
88	GAM11	A3	RW	Gamma Curve 11th Segment Input End Point 0x60 Output Value
89	GAM12	AF	RW	Gamma Curve 12th Segment Input End Point 0x70 Output Value
8A	GAM13	C4	RW	Gamma Curve 13th Segment Input End Point 0x90 Output Value
8B	GAM14	D7	RW	Gamma Curve 14th Segment Input End Point 0xB0 Output Value
8C	GAM15	E8	RW	Gamma Curve 15th Segment Input End Point 0xD0 Output Value
8D	SLOP	20	RW	Gamma Curve Highest Segment Slope - calculated as follows: SLOP[7:0] = (0x100 - GAM15[7:0]) x 4/3
8E	DNSTh	00	RW	De-noise Threshold

Table 6 Device Control Register List (Sheet 10 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
8F	EDGE0	00	RW	Edge Enhancement Control 0 Bit[7:5]: Reserved Bit[4:0]: Edge enhancement strength control
90	EDGE1	08	RW	Edge Enhancement Control 1 Bit[7:4]: Reserved Bit[3:0]: Edge enhancement threshold control
91	DNSOff	10	RW	Auto De-noise Threshold Control
92	EDGE2	1F	RW	Edge Enhancement Strength Low Point Control
93	EDGE3	01	RW	Edge Enhancement Strength High Point Control
94	MTX1	2C	RW	Matrix Coefficient 1
95	MTX2	24	RW	Matrix Coefficient 2
96	MTX3	08	RW	Matrix Coefficient 3
97	MTX4	14	RW	Matrix Coefficient 4
98	MTX5	24	RW	Matrix Coefficient 5
99	MTX6	38	RW	Matrix Coefficient 6
9A	MTX_Ctrl	9E	RW	Matrix Control Bit[7]: Matrix double ON/OFF selection Bit[6]: Reserved Bit[5]: Sign bit for MTX6 Bit[4]: Sign bit for MTX5 Bit[3]: Sign bit for MTX4 Bit[2]: Sign bit for MTX3 Bit[1]: Sign bit for MTX2 Bit[0]: Sign bit for MTX1
9B	BRIGHT	00	RW	Brightness Control
9C	CNST	40	RW	Contrast Control
9D	CNST_ctr	00	RW	Contrast Control Center
9E	UVADJ0	11	RW	Auto UV Adjust Control 0 Bit[7:4]: Auto UV adjust offset control 4 LSBs Bit[3:0]: Auto UV adjust threshold control
9F	UVADJ1	02	RW	Auto UV Adjust Control 1 Bit[7:3]: Auto UV adjust value Bit[2]: Reserved Bit[1]: Auto UV adjust stop control Bit[0]: Auto UV adjust offset control MSB
A0	SCAL0	00	RW	Scaling Control 0
A1	SCAL1	40	RW	Scaling Control 1 – for horizontal scaling control
A2	SCAL2	40	RW	Scaling Control 2 – for vertical scaling control
A3	FIFOdlyM	06	RW	FIFO Manual Mode Delay Control
A4	FIFOdlyA	00	RW	FIFO Auto Mode Delay Control

Table 6 Device Control Register List (Sheet 11 of 11)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
A5	RSVD	XX	–	Reserved
A6	SDE	00	RW	Special Digital Effect Control
A7	USAT	40	RW	U Component Saturation Control
A8	VSAT	40	RW	V Component Saturation Control
A9	HUE0	80	RW	Hue Control 0
AA	HUE1	80	RW	Hue Control 1
AB	SIGN	06	RW	Sign Bit for Hue and Contrast Bit[7:4]: Reserved Bit[3:2]: Contrast sign bit Bit[1:0]: Hue sign bit
AC	DSPAuto	FF	RW	DSP Auto Function ON/OFF Control Bit[7]: AWB auto threshold control Bit[6]: De-noise auto threshold control Bit[5]: Edge enhancement auto strength control Bit[4]: UV adjust auto slope control Bit[3]: Auto scaling factor control (register SCAL0 (0xA0)) Bit[2]: Auto scaling factor control (registers SCAL1 (0xA1 and SCAL2 (0xA2)) Bit[1:0]: Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7725 uses a 28-ball Chip Scale Package 2 (CSP2). Refer to Figure 12 for package information, Table 7 for package dimensions and Figure 13 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 12 OV7725-CSP2 Package Specifications

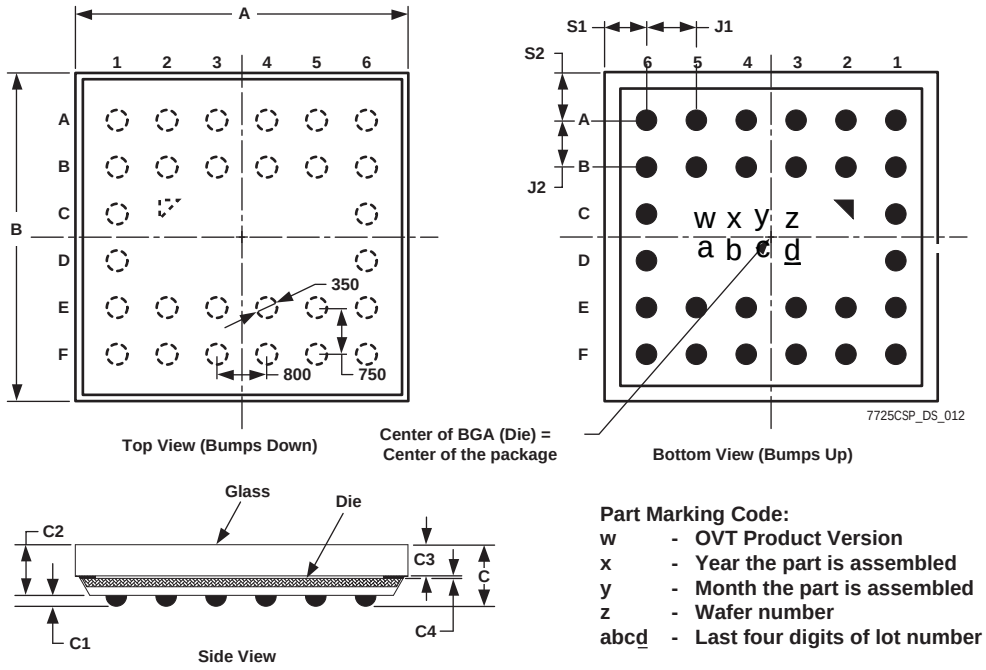
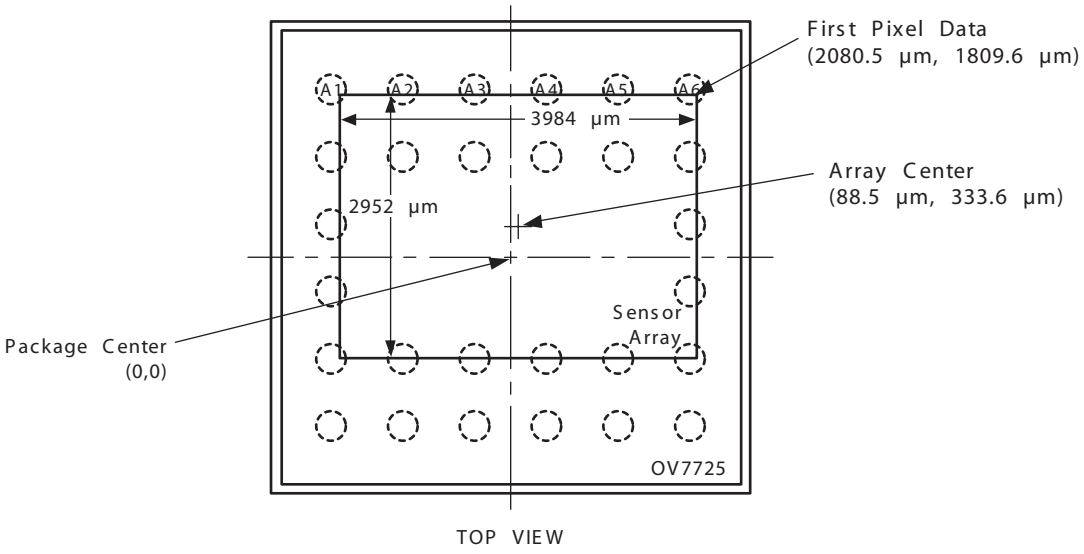


Table 7 OV7725-CSP2 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package Body Dimension X	A	5320	5345	5370	µm
Package Body Dimension Y	B	5240	5265	5290	µm
Package Height	C	845	905	965	µm
Ball Height	C1	150	180	210	µm
Package Body Thickness	C2	680	725	770	µm
Cover Glass Thickness	C3	375	400	425	µm
Airgap Between Cover Glass and Sensor	C4	30	45	60	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		28		
Pin Count X-axis	N1		6		
Pin Count Y-axis	N2		6		
Pins Pitch X-axis	J1		800		µm
Pins Pitch Y-axis	J2		750		µm
Edge-to-Pin Center Distance Analog X	S1	643	673	703	µm
Edge-to-Pin Center Distance Analog Y	S2	728	758	788	µm

Sensor Array Center

Figure 13 OV7725 Sensor Array Center



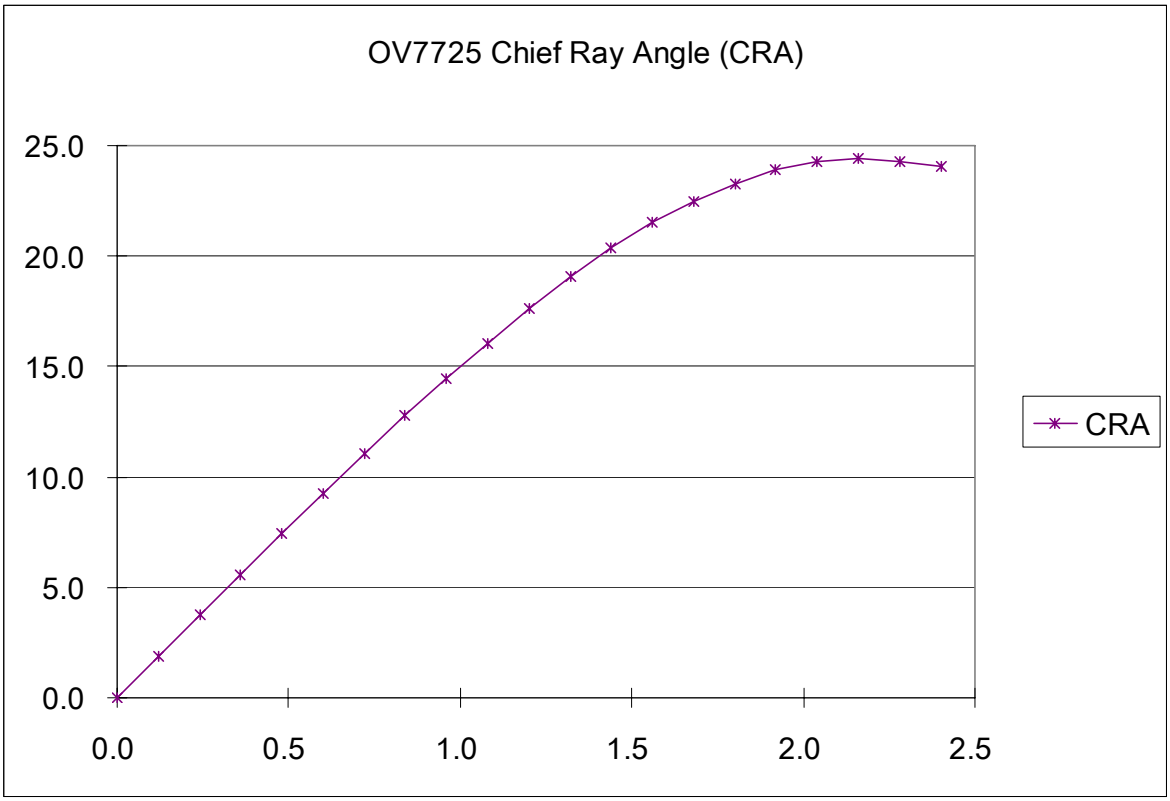
NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

7725CSP_DS_013

Chief Ray Angle

Figure 14 OV7725 Chief Ray Angle



IR Reflow Ramp Rate Requirements

OV7725 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 15 IR Reflow Ramp Rate Requirements

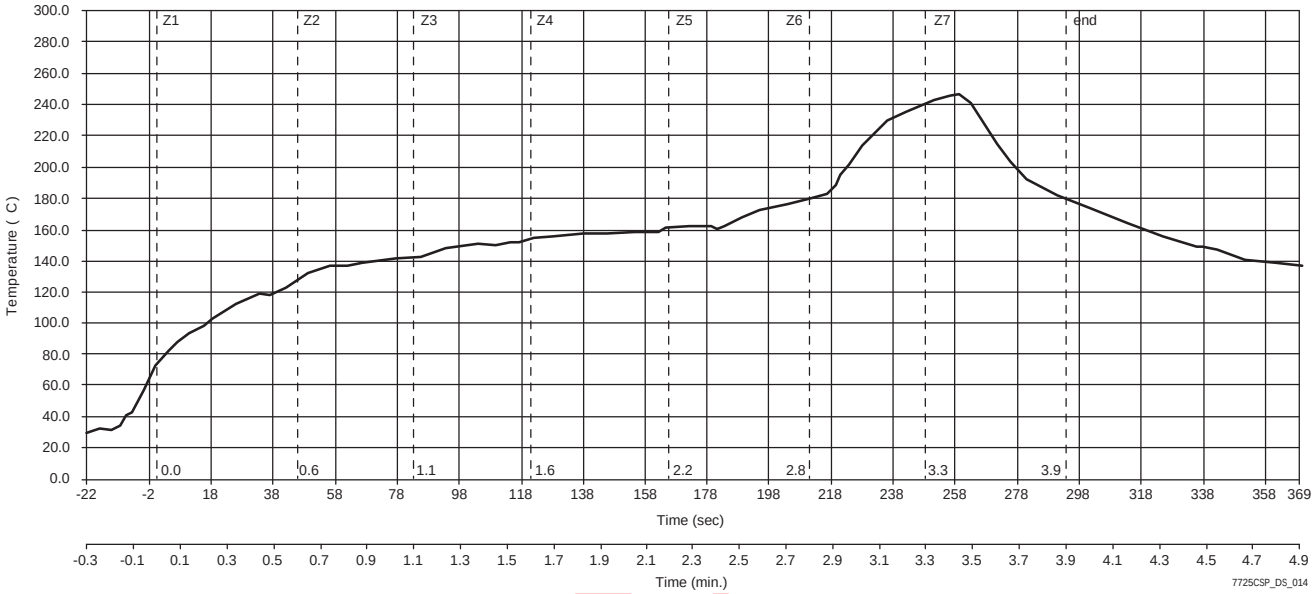


Table 8 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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