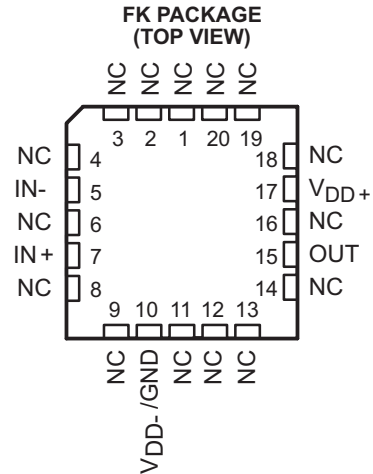


CLASS V, ADVANCED LinCMOS™ LOW NOISE PRECISION OPERATIONAL AMPLIFIER

Check for Samples: [TLC2201-SP](#)

FEATURES

- QML-V Qualified SMD 5962-9088203V2A
- Low Input Offset Voltage: 400 μV Max
- Excellent Offset Voltage Stability With Temperature: 0.5 $\mu\text{V}/^\circ\text{C}$ Typ
- Rail-to-Rail Output Swing
- Low Input Bias Current: 1 pA Typ at $T_A = 25^\circ\text{C}$
- Common-Mode Input Voltage Range Includes the Negative Rail
- Fully Specified For Both Single-Supply and Split-Supply Operation



NC - No internal connection

DESCRIPTION

The TLC2201 is a precision, low-noise operational amplifier using Texas Instruments Advanced LinCMOS™ process. This device combines the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS™ process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The combination of excellent DC and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal-conditioning applications in either single-supply or split-supply configurations.

The device inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the parametric performance.

The TLC2201 is characterized for operation over the full military temperature range of -55°C to 125°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinCMOS is a trademark of Texas Instruments.

Parts, PSpice are trademarks of MicroSim Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

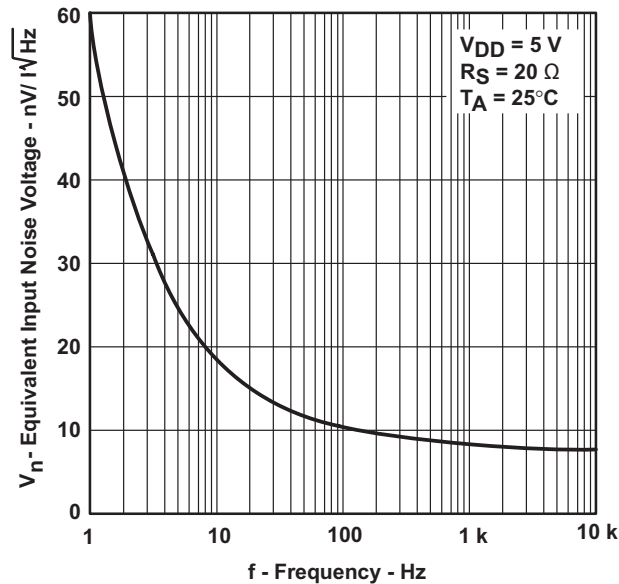
© 2011, Texas Instruments Incorporated



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**TYPICAL EQUIVALENT
INPUT NOISE VOLTAGE
vs
FREQUENCY**

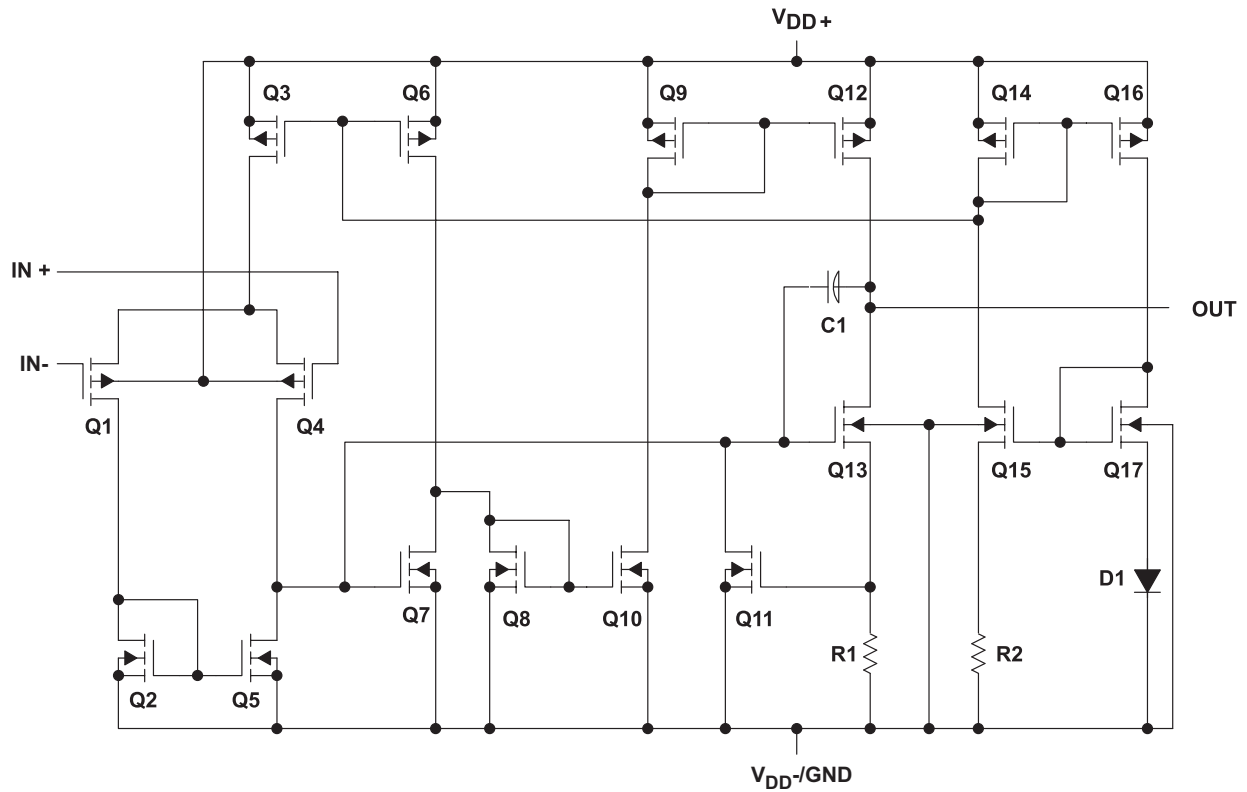


ORDERING INFORMATION⁽¹⁾

TEMPERATURE	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C T _{case}	20-pin FK	5962-9088203V2A	5962-9088203V2A TLC2201AMFKBQMLV

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

EQUIVALENT SCHEMATIC



ACTUAL DEVICE COMPONENT COUNT	
COMPONENT	TLC2201
Transistors	17
Resistors	2
Diodes	1
Capacitors	1

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
V _{DD}	Supply voltage ⁽²⁾ , V _{DD-} to V _{DD+}	-8 to 8	V
V _{ID}	Differential input voltage ⁽³⁾	±16	V
V _I	Input voltage (any input)	±8	V
I _I	Input current (each input)	±5	mA
I _O	Output current (each output)	±50	mA
	Duration of short-circuit current at (or below) 25°C ⁽⁴⁾	Unlimited	
	Continuous total power dissipation	See Dissipation Ratings Table	
T _C	Operating case temperature	-55 to 125	°C
T _{stg}	Storage temperature	-65 to 150	°C
	Case temperature for 60 seconds	260	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential voltages are with respect to the midpoint between V_{DD+} and V_{DD-}.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

THERMAL RESISTANCE FOR FK PACKAGE⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-case thermal resistance			16	°C/W

- (1) Maximum power dissipation is a function of T_J (max), θ_{JC} and T_C. The maximum allowable power dissipation at any allowable case temperature is PD = (T_J (max) - T_C)/θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (2) The package thermal impedance is calculated in accordance with MIL-STD-883.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{DD±}	Supply voltage	±2.3	±8	V
V _{IC}	Common-mode input voltage	V _{DD-}	V _{DD+} -2.3	V
T _C	Operating case temperature	-55	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT			
V_{IO}	Input offset voltage	$V_{IC} = 0,$ $R_S = 50\ \Omega$	25°C		80	200	μV			
			Full range			400				
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		$\mu\text{V}/^\circ\text{C}$			
	Input offset voltage long-term drift ⁽²⁾		25°C		0.001		$\mu\text{V}/\text{mo}$			
I_{IO}	Input offset current		25°C		0.5		pA			
			Full range			500				
I_{IB}	Input bias current		25°C		1		pA			
			Full range			500				
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	0 to 2.7			V			
V_{OH}	Maximum high-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4.7	4.8		V			
			Full range	4.7						
V_{OL}	Maximum low-level output voltage		$I_O = 0$	25°C		0	50	mV		
			Full range				50			
A_{VD}	Large-signal differential voltage amplification		$V_O = 1\ \text{V to } 4\ \text{V},$ $R_L = 500\ \text{k}\Omega$	25°C	150	315		V/mV		
				Full range	75					
				25°C	$V_O = 1\ \text{V to } 4\ \text{V},$ $R_L = 10\ \text{k}\Omega$	25	55			
						Full range	10			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin},$ $V_O = 0,$ $R_S = 50\ \Omega$	25°C	90	110		dB			
			Full range	85						
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)		$V_{DD} = 4.6\ \text{V to } 16\ \text{V}$	25°C	90	110		dB		
				Full range	85					
I_{DD}	Supply current			$V_O = 2.5\ \text{V},$ No load	25°C		1.1	1.5	mA	
					Full range					1.5
SR	Slew rate at unity gain				$V_O = 0.5\ \text{V to } 2.5\ \text{V},$ $R_L = 10\ \text{k}\Omega$ $C_L = 100\ \text{pF}$	25°C	1.8	2.5		V/ μs
						Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz				25°C		18		nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz				25°C		8		
$V_{n(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C				0.5		μV	
		f = 0.1 to 10 Hz	25°C				0.7			
I_n	Equivalent input noise current		25°C			0.6		fA/ $\sqrt{\text{Hz}}$		
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ \text{k}\Omega,$ $C_L = 100\ \text{pF}$	25°C			1.8		MHz		
Φ_m	Phase margin at unity gain	$R_L = 10\ \text{k}\Omega,$ $C_L = 100\ \text{pF}$	25°C		45°					

(1) Full range is -55°C to 125°C .

(2) Typical values are based on the input offset voltage shift observable through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{DD} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT		
V_{IO}	Input offset voltage	$V_{IC} = 0,$ $R_S = 50\ \Omega$	25°C		80	200	μV		
			Full range			400			
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		$\mu\text{V}/^\circ\text{C}$		
	Input offset voltage long-term drift ⁽²⁾		25°C		0.001		$\mu\text{V}/\text{mo}$		
I_{IO}	Input offset current		25°C		0.5		pA		
			Full range			500			
I_{IB}	Input bias current		25°C		1		pA		
			Full range			500			
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	Full range	-5 to 2.7			V		
V_{OM+}	Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	4.7	4.8		V		
			Full range	4.7					
V_{OM-}	Maximum negative peak output voltage swing		25°C	-4.7	-4.9		V		
			Full range	-4.7					
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 4\ \text{V},$ $R_L = 500\ \text{k}\Omega$	25°C	400	560		V/mV	
				Full range	200				
				25°C	$V_O = \pm 4\ \text{V},$ $R_L = 10\ \text{k}\Omega$	90	100		
						Full range	45		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin},$ $V_O = 0,$ $R_S = 50\ \Omega$	25°C	90	115		dB		
			Full range	85					
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = \pm 2.3\ \text{V to } \pm 8\ \text{V}$	25°C	90	110		dB		
			Full range	85					
I_{DD}	Supply current	$V_O = 0\ \text{V},$ No load	25°C		1.1	1.5	mA		
			Full range			1.5			
SR	Slew rate at unity gain	$V_O = \pm 2.3\ \text{V},$ $R_L = 10\ \text{k}\Omega$ $C_L = 100\ \text{pF}$	25°C	2	2.7		V/ μs		
			Full range	1.3					
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		$\text{nV}/\sqrt{\text{Hz}}$		
		f = 1 kHz	25°C		8				
$V_{n(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV		
		f = 0.1 to 10 Hz	25°C		0.7				
I_n	Equivalent input noise current		25°C		0.6		$\text{fA}/\sqrt{\text{Hz}}$		
	Gain-bandwidth product	f = 10 kHz, $R_L = 10\ \text{k}\Omega,$ $C_L = 100\ \text{pF}$	25°C		1.9		MHz		
Φ_m	Phase margin at unity gain	$R_L = 10\ \text{k}\Omega,$ $C_L = 100\ \text{pF}$	25°C		48°				

(1) Full range is -55°C to 125°C .

(2) Typical values are based on the input offset voltage shift observable through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

PARAMETER MEASUREMENT INFORMATION

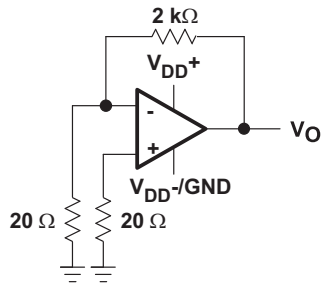
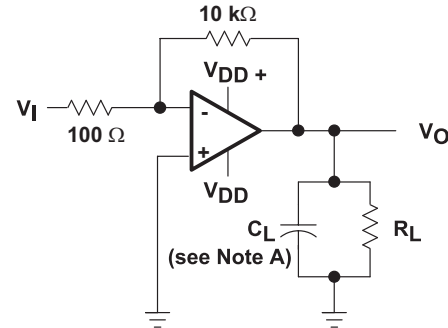
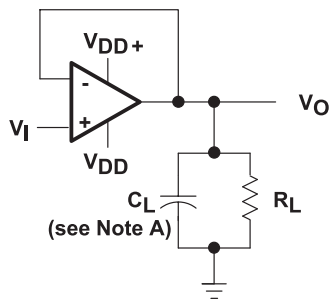


Figure 1. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 2. Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Slew-Rate Test Circuit

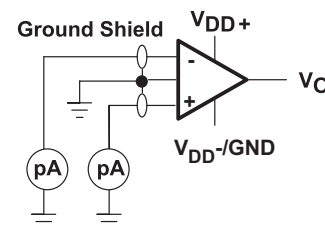


Figure 4. Input-Bias and Offset-Current Test Circuit

TYPICAL VALUES

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

INPUT BIAS AND OFFSET CURRENT

At the picoamp bias current level of the TLC2201 accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket, and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

NOISE

Texas Instruments offers automated production noise testing to meet individual application requirements. Noise voltage at $f = 10$ Hz and $f = 1$ kHz is sample tested on every TLC2201. For other noise requirements, please contact the factory.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	Figure 5
I_{IB}	Input bias current	vs Common-mode input voltage	Figure 6
		vs Free-air temperature	Figure 7
V_{OM}	Maximum peak output voltage	vs Output curre	Figure 8
		vs Free-air temperature	Figure 9
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	Figure 10
V_{OH}	High-level output voltage	vs Frequency	Figure 11
		vs High-level output current	Figure 12
		vs Free-air temperature	Figure 13
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 14
		vs Free-air temperature	Figure 15
A_{VD}	Large-signal differential voltage amplification	vs Frequency	Figure 16
		vs Free-air temperature	Figure 17
I_{OS}	Short-circuit output current	vs Supply voltage	Figure 18
		vs Free-air temperature	Figure 19
CMRR	Common-mode rejection ratio	vs Frequency	Figure 20
I_{DD}	Supply current	vs Supply voltage	Figure 21
		vs Free-air temperature	Figure 22
	Pulse response	Small signal	Figure 23
			Figure 24
		Large signal	Figure 25
			Figure 26
SR	Slew rate	vs Supply voltage	Figure 27
		vs Free-air temperature	Figure 28
	Noise voltage (referred to input)	0.1 Hz to 1 Hz	Figure 29
		0.1 Hz to 10 Hz	Figure 30
	Gain-bandwidth product	vs Supply voltage	Figure 31
		vs Free-air temperature	Figure 32
Φ_m	Phase margin	vs Supply voltage	Figure 33
		vs Free-air temperature	Figure 34
	Phase shift	vs Frequency	Figure 16

TYPICAL CHARACTERISTICS

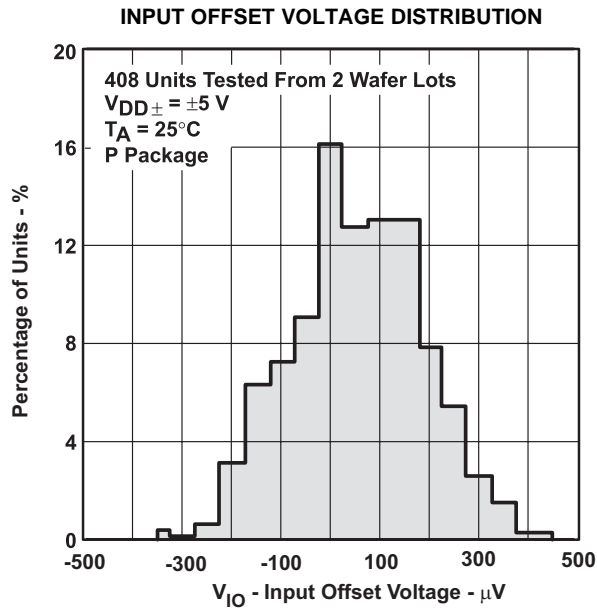


Figure 5.

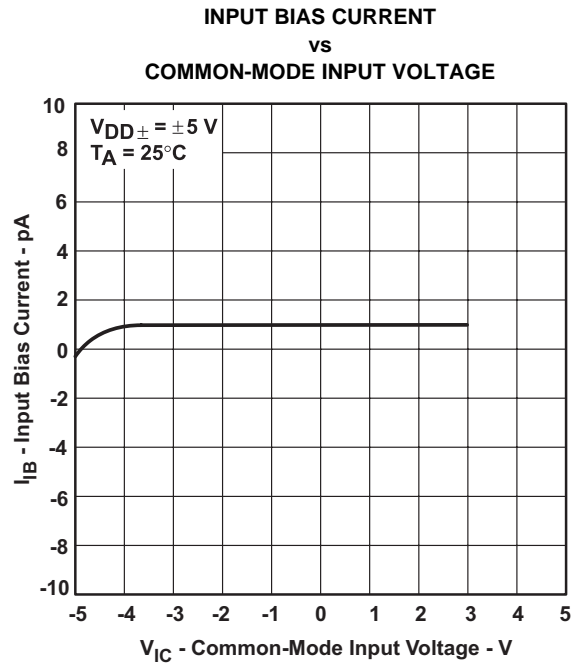


Figure 6.

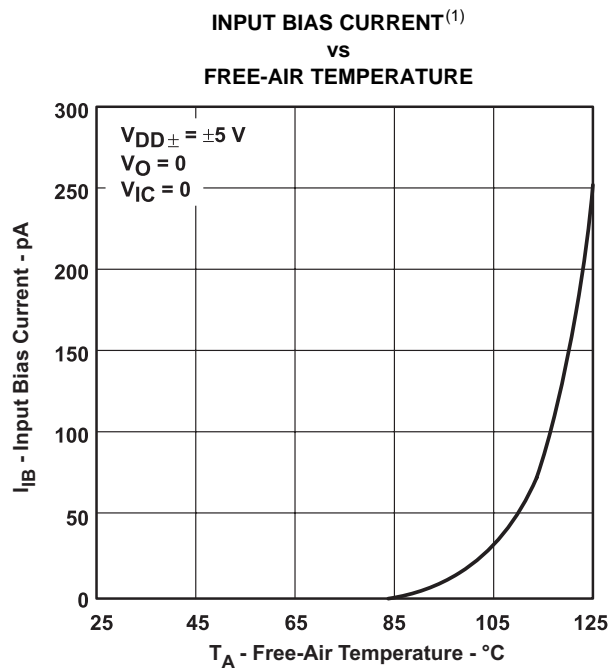


Figure 7.

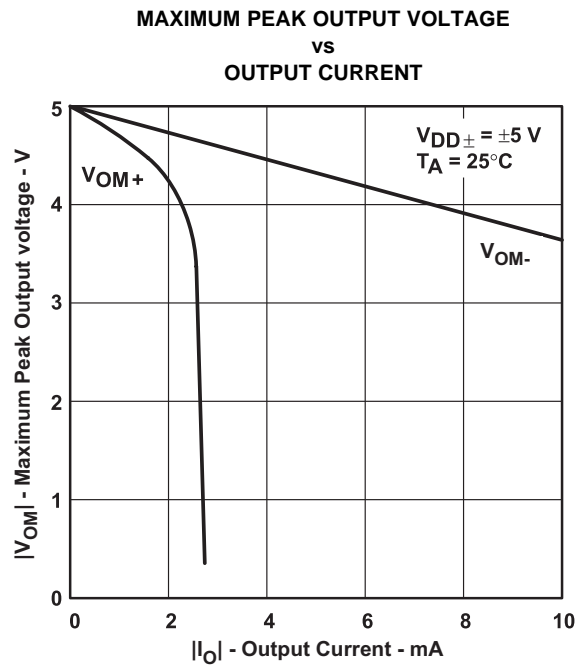


Figure 8.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (continued)

**MAXIMUM PEAK OUTPUT VOLTAGE⁽²⁾
vs
FREE-AIR TEMPERATURE**

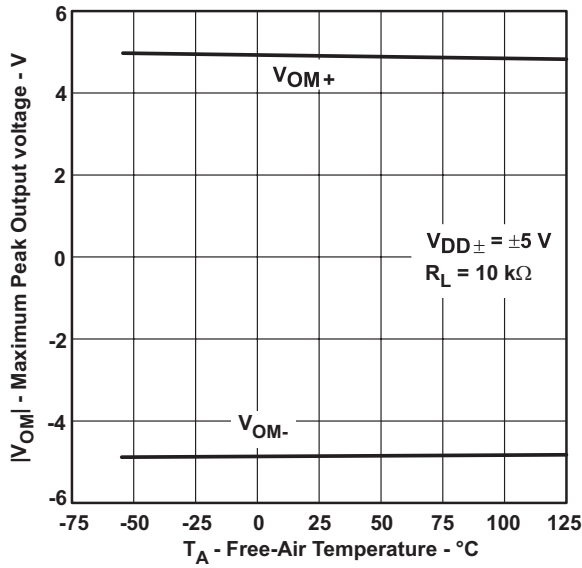


Figure 9.

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

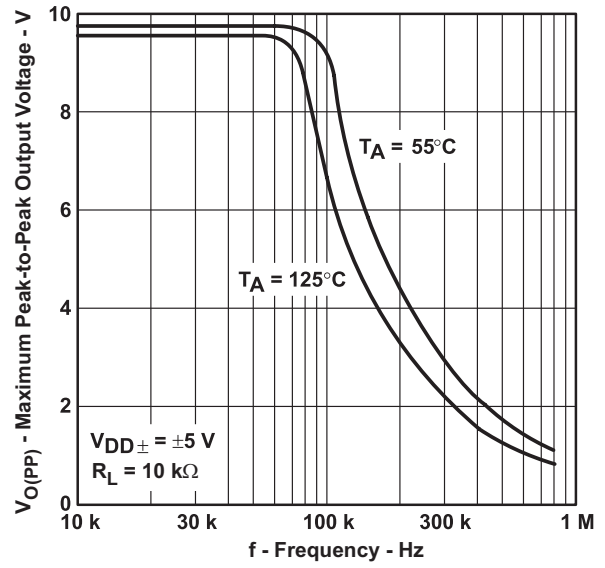


Figure 10.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY**

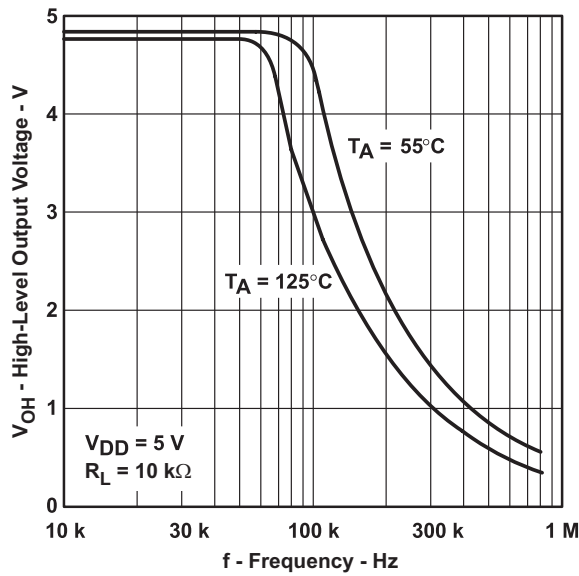


Figure 11.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

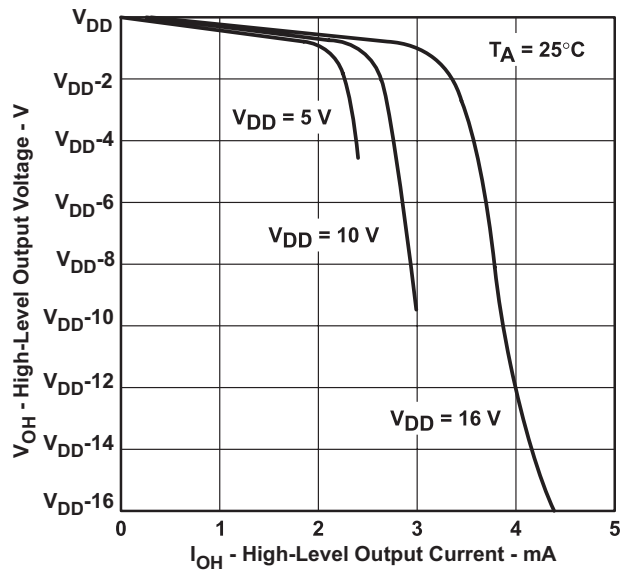


Figure 12.

(2) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

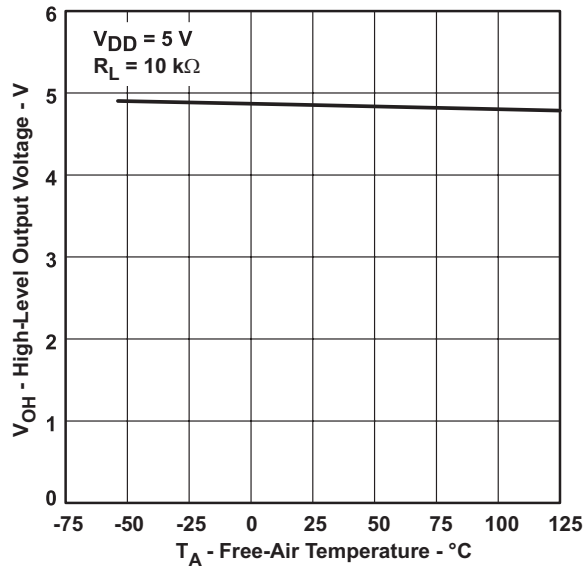


Figure 13.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

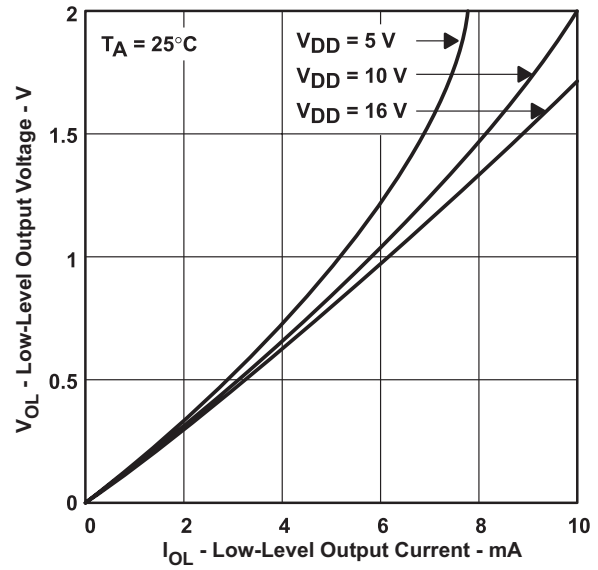


Figure 14.

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

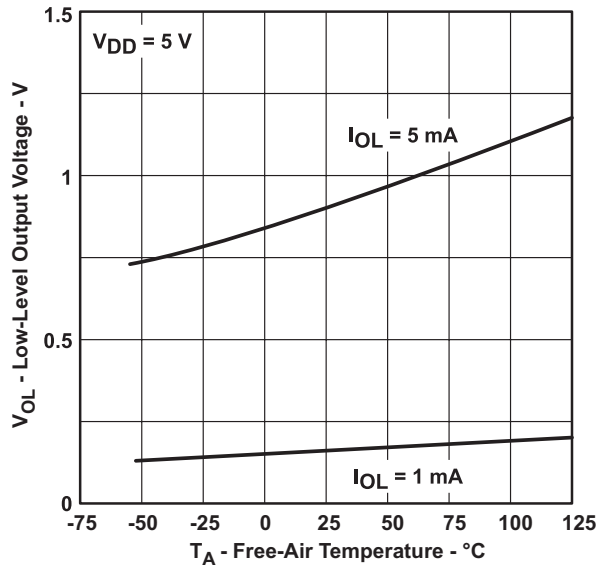


Figure 15.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

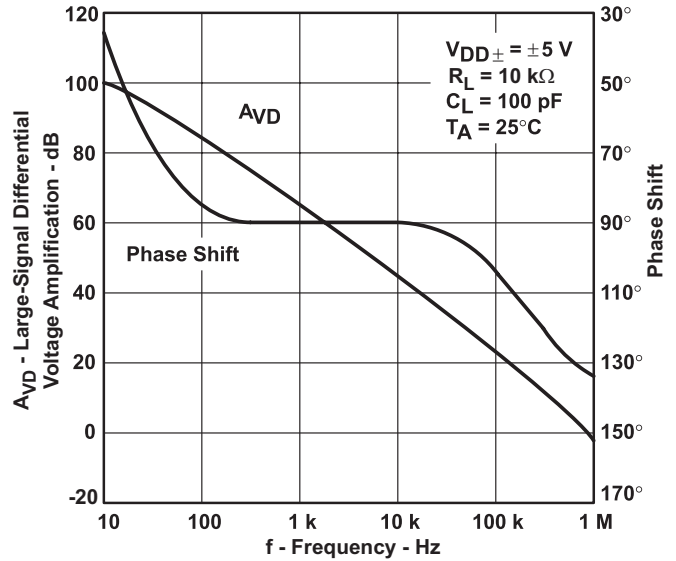


Figure 16.

TYPICAL CHARACTERISTICS (continued)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION

vs
FREE-AIR TEMPERATURE

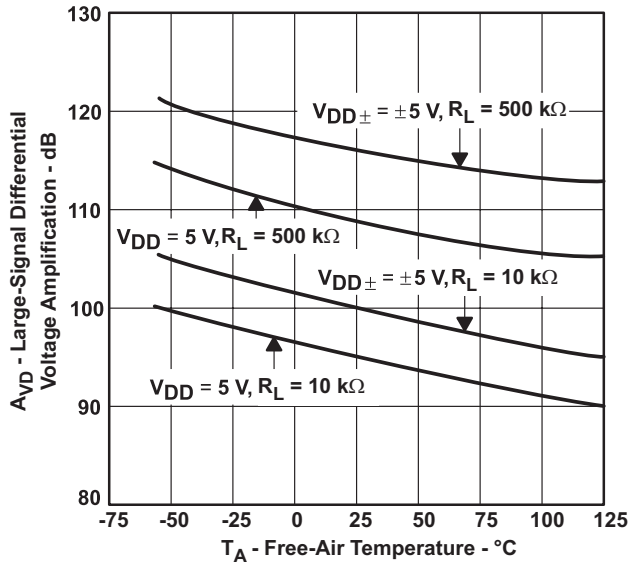


Figure 17.

SHORT-CIRCUIT OUTPUT CURRENT

vs
SUPPLY VOLTAGE

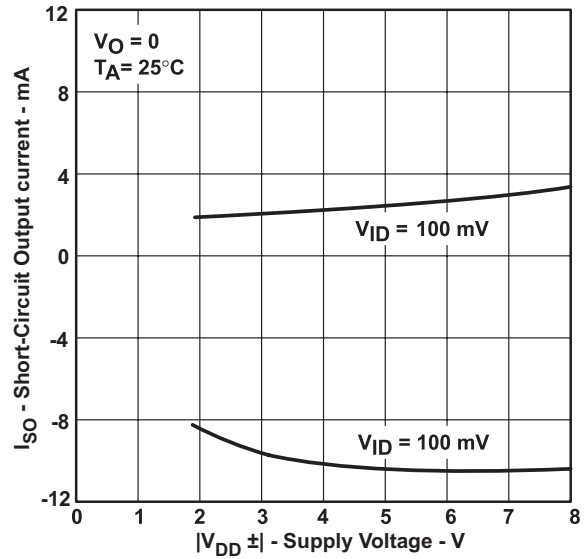


Figure 18.

SHORT-CIRCUIT OUTPUT CURRENT

vs
FREE-AIR TEMPERATURE

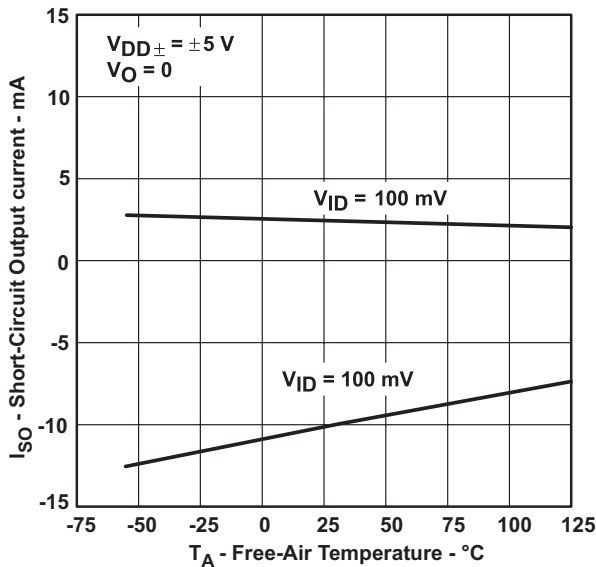


Figure 19.

COMMON-MODE REJECTION RATIO

vs
FREQUENCY

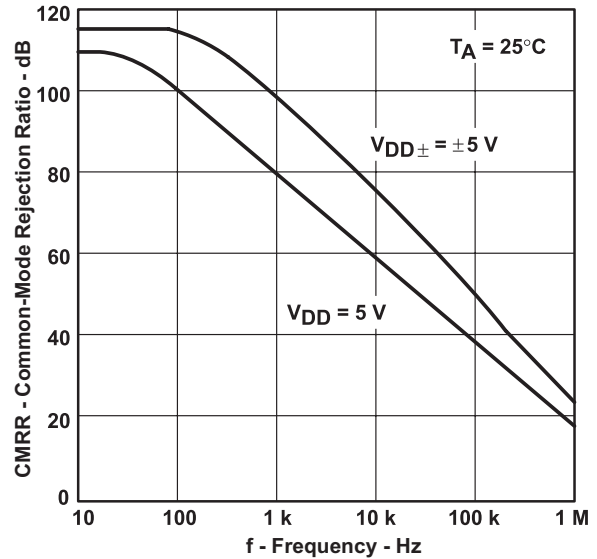


Figure 20.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

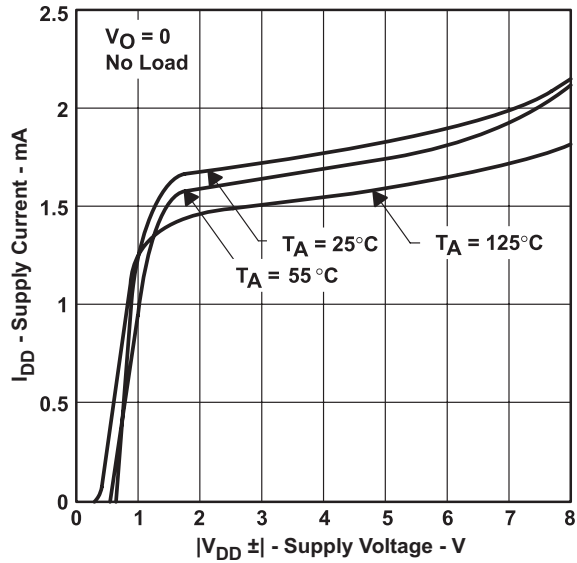


Figure 21.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

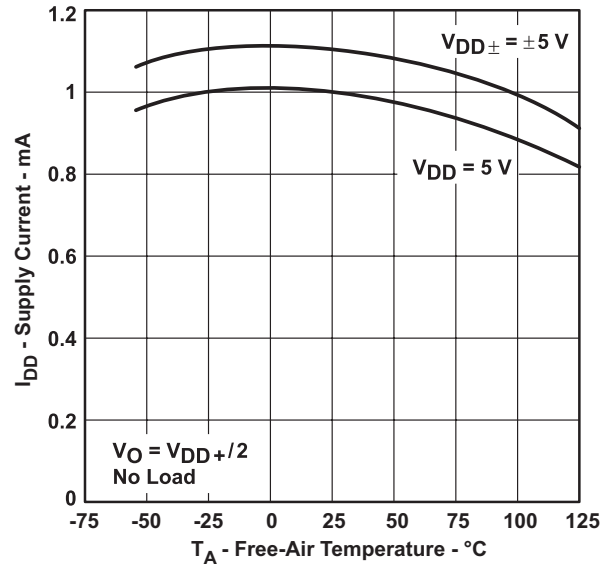


Figure 22.

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

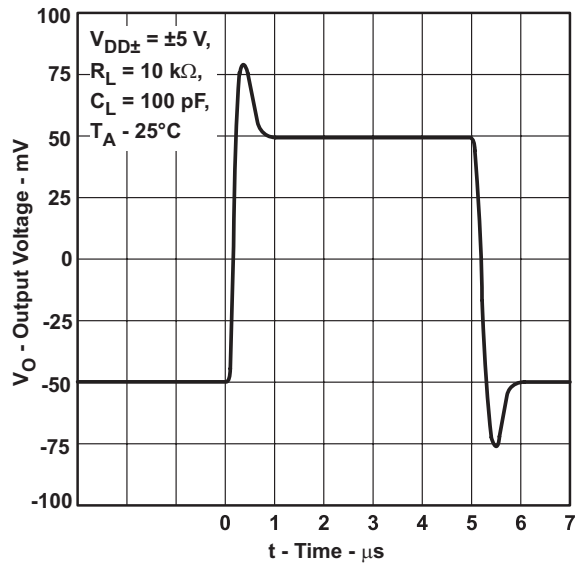


Figure 23.

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

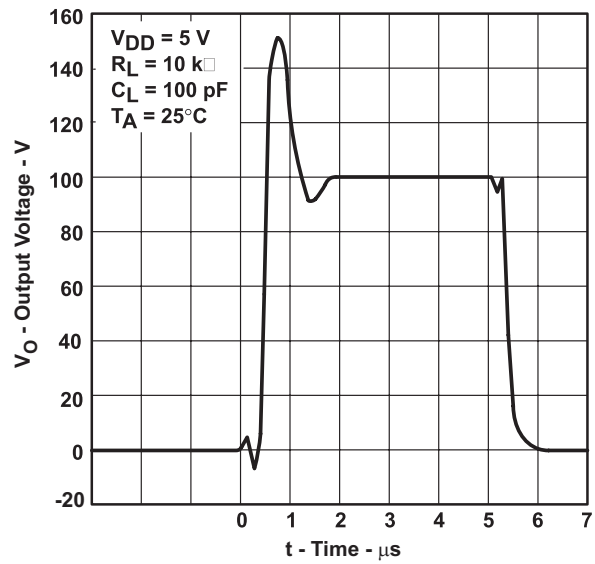


Figure 24.

TYPICAL CHARACTERISTICS (continued)

**VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE**

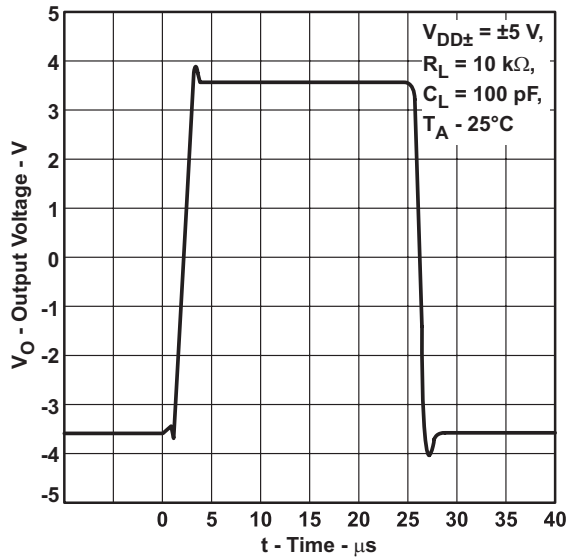


Figure 25.

**VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE**

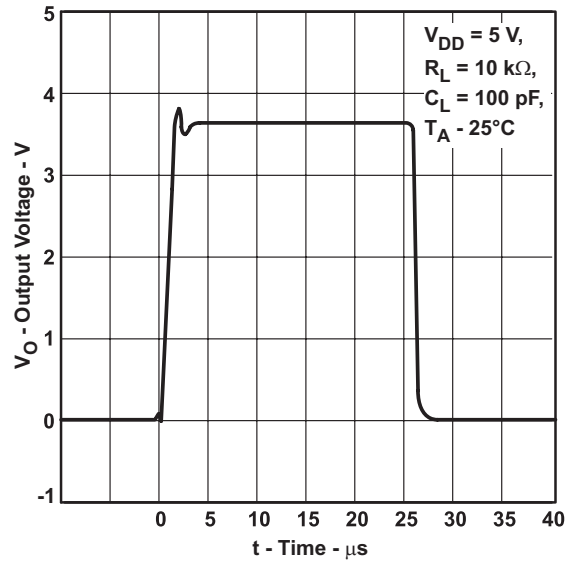


Figure 26.

**SLEW RATE
vs
SUPPLY VOLTAGE**

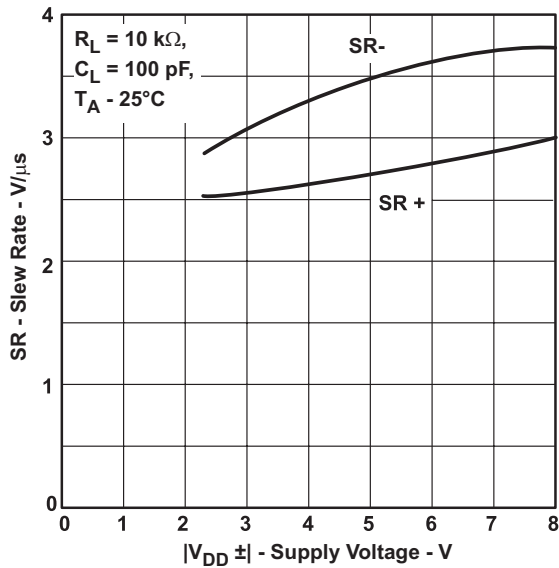


Figure 27.

**SLEW RATE
vs
FREE-AIR TEMPERATURE**

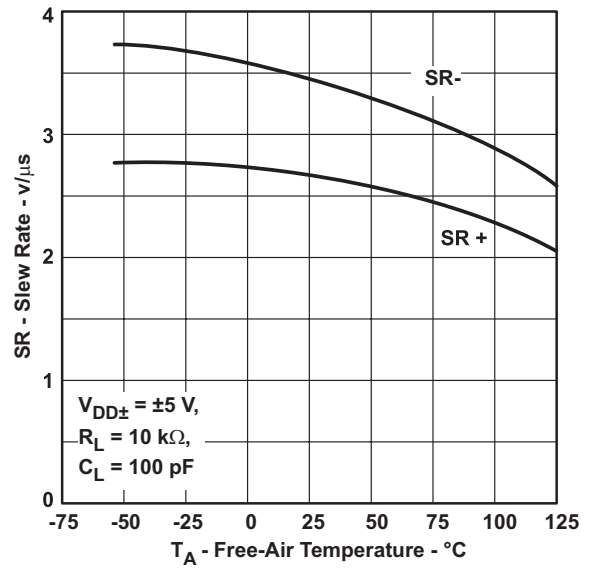


Figure 28.

TYPICAL CHARACTERISTICS (continued)

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

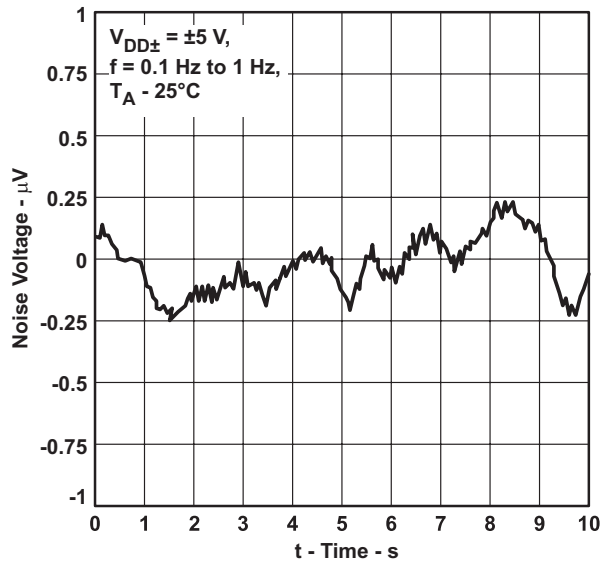


Figure 29.

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

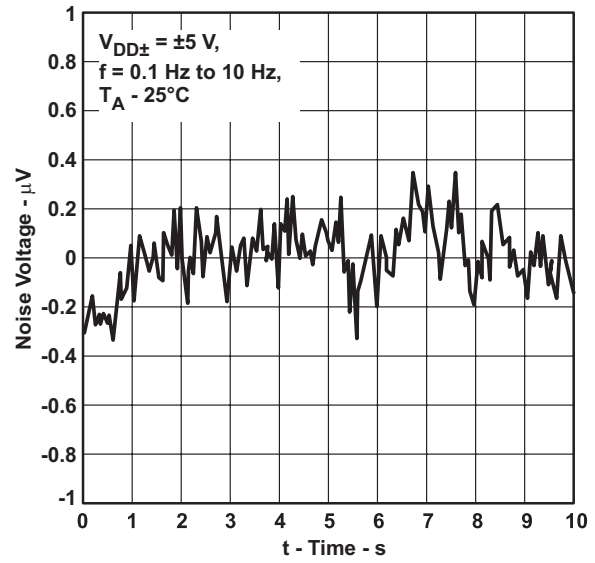


Figure 30.

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

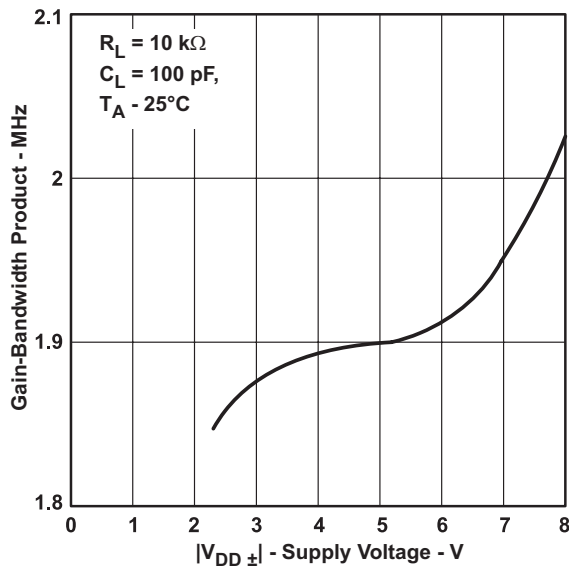


Figure 31.

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

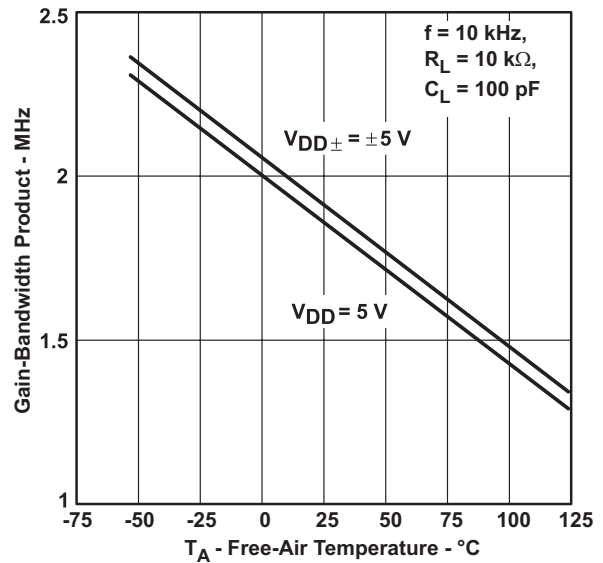


Figure 32.

TYPICAL CHARACTERISTICS (continued)

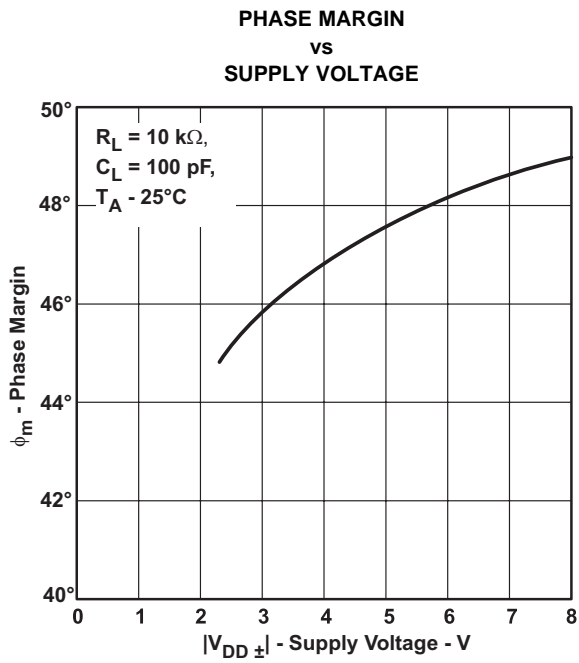


Figure 33.

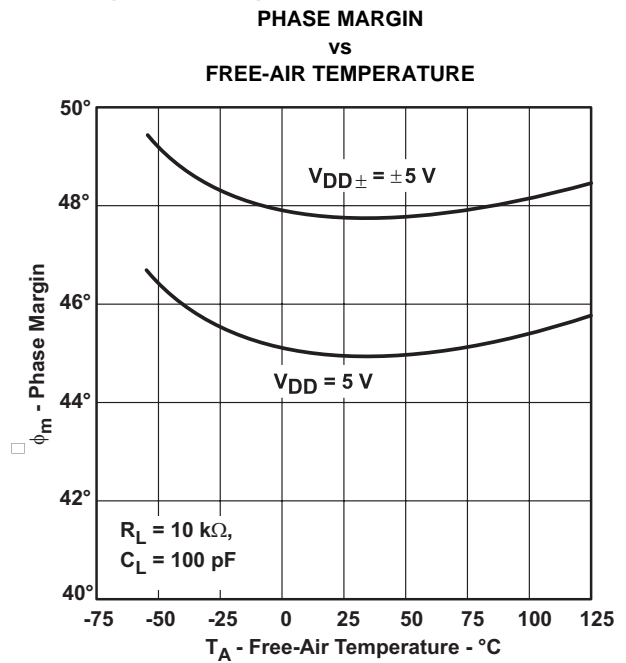


Figure 34.

APPLICATION INFORMATION

LATCH-UP AVOIDANCE

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2201 inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques reducing the chance of latch-up should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

ELECTROSTATIC DISCHARGE PROTECTION

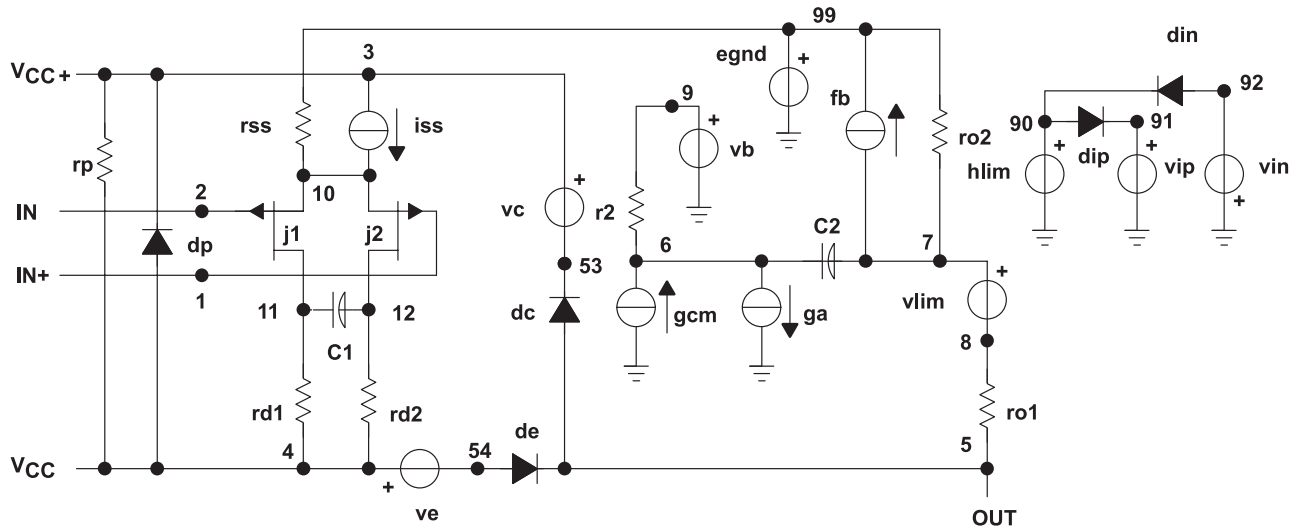
These devices use internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

MACROMODEL INFORMATION

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel⁽³⁾ and subcircuit in [Figure 35](#) were generated using the TLC2201 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(3) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).



```

.subckt TLC220x 1 2 3 4 5
*
c1 11 12 8.51E12
c2 6 7 50.00E12
cpsr 85 86 79.6E9
dcm+ 81 82 dx
dcm 83 81 dx
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
ecmr 84 99 (2,99) 1
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
epsr 85 0 poly(1) (3,4) 200E6 20E6
ense 89 2 poly(1) (88,0) 100E6 1
fb 7 99 poly(6) vb vc ve vlp vln
+ vpsr 0 + 895.9E3 90E3 90E3 90E3 90E3 895E3
ga 6 0 11 12 314.2E6
gcm 0 6 10 99 1.295E9
gpsr 85 86 (85,86) 100E6
grd1 60 11 (60,11) 3.141E4
grd2 60 12 (60,12) 3.141E4
hlim 90 0 vlim 1k
hcmr 80 1 poly(2) vcm+ vcm 0 1E2 1E2
irp 3 4 965E6

iss 3 10 dc 135.0E6
iio 2 0 .5E12
i1 88 0 1E21
j1 11 89 10 jx
j2 12 80 10 jx
r2 6 9 100.0E3
rcm 84 81 1k
rn1 88 0 1500
ro1 8 5 188
ro2 7 99 187
rss 10 99 1.481E6
vad 60 4 .3v
vcm+ 82 99 2.2
vcm 83 99 4.5
vb 9 0 dc 0
vc 3 53 dc .9
ve 54 4 dc .8
vlim 7 8 dc 0
vlp 91 0 dc 2.8
vln 0 92 dc 2.8
vpsr 0 86 dc 0
.model dx d(is=800.0E18)
.model jx pjf(is=500.0E15 beta=1.462E3
+ vto=.155 kf=1E17)
.endsx
    
```

Figure 35. Boyle Macromodel and Subcircuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9088203V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TLC2201-SP :

● Catalog: [TLC2201](#)

● Military: [TLC2201M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

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