XM-04

Bluetooth Module

Hardware

Datasheet

Rev 1.1

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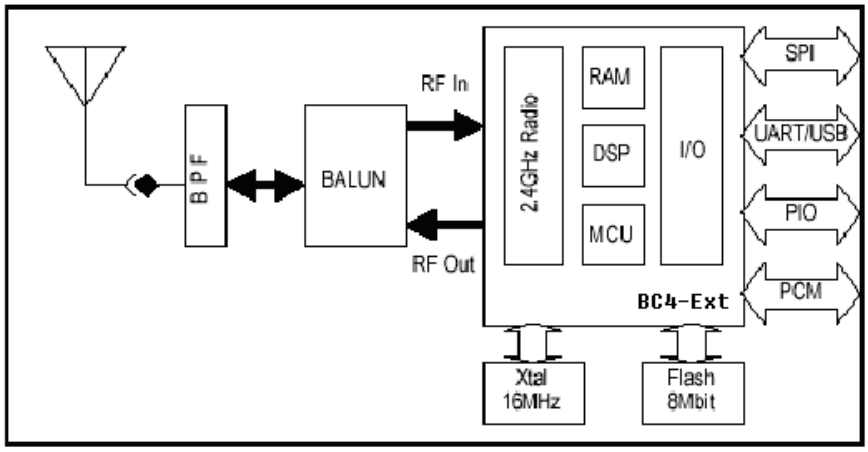
2. Product Description

The BC04 Bluetooth Module is a Class 2 Bluetooth module using BlueCore4-External chipset from leading Bluetooth chipset supplier, Cambridge Silicon Radio. It provides a fully compliant Bluetooth system for data and voice communications. Interfaces with a host via USB or UART and support full data rate up to 3Mbps modulation modes. Voice interface supported PCM protocol. The module and device firmware is fully compliant with the Bluetooth specification v2.1+EDR.

3. Applications

3.1 PCs, PDAs
3.2 Computer Accessories (CF Cards, USB Dongles, PCMCIA, RS232 Adaptors, etc.)
3.3 Mice, Keyboard, Joysticks
3.4 Cordless Phone
3.5 FAX, Printer Adaptors
3.6 Digital Camera
3.7 Access Points to LAN and/or Dial-up network

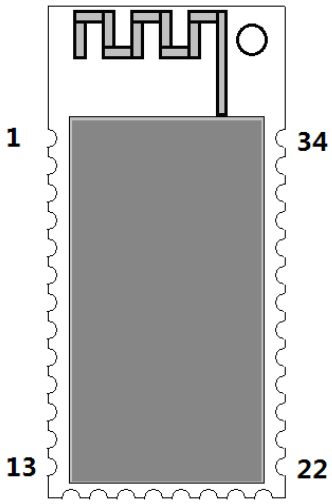
4. Block Diagram



5. Pin Descriptions

5.1 Device Terminal

No.	Des		Des	No.
1	UART_TX		PIO11	34
2	UART_RX		PIO10	33
3	UART_CTS		PIO9	32
4	UART_RTS		PIO8	31
5	PCM_CLK		PIO7	30
6	PCM_OUT		PIO6	29
7	PCM_IN		PIO5	28
8	PCM_SYNC		PIO4	27
9	AIO0		PIO3	26
10	AIO1		PIO2	25
11	RESETB		PIO1	24
12	VCC		PIO0	23
13	GND		GND	22



14	15	16	17	18	19	20	21
1V8	USB_D-	SPI_CSB	SPI_MOSI	SPI_MISO	SPI_CLK	USB_D+	GND

5.2 Device Terminal Functions

Pin	NAME	I/O Type	DESCRIPTION
1	UART_TXD	O	UART data output
2	UART_RXD	I	UART data input
3	UART_CTS	I	UART clear to send active low
4	UART_RTS	O	UART request to send active low
5	PCM_CLK	I	Synchronous data clock
6	PCM_OUT	O	Synchronous data data out

7	PCM_IN	I	Synchronous data data in
8	PCM_SYNC	I	Synchronous data sync
9	AIO0	I/O	Programmable input/output line
10	AIO1	I/O	Programmable input/output line
11	RESETB	I	Integrated inside the RC reset circuit, Reset if low. Input debounced so must be low for >5ms to cause a reset
12	VCC	S	Power Supply
13	GND	S	Ground
14	1V8	S	Filter Capacitor for 1.8V
15	USB_D-	I/O	USB data minus
16	SPI_CSB	I/O	Chip select for Synchronous Serial Interface active low
17	SPI_MOSI	I/O	Serial Peripheral Interface data input
18	SPI_MISO	I/O	Serial Peripheral Interface data output
19	SPI_CLK	I/O	Serial Peripheral Interface clock
20	USB_D+	I/O	USB data plus with selectable internal 1.5k. pull-up resistor
21	GND		Ground
22	GND		Ground
23	PIO0	I/O	Programmable input/output line
24	PIO1	I/O	Programmable input/output line
25	PIO2	I/O	Programmable input/output line
26	PIO3	I/O	Programmable input/output line
27	PIO4	I/O	Programmable input/output line
28	PIO5	I/O	Programmable input/output line
29	PIO6	I/O	Programmable input/output line
30	PIO7	I/O	Programmable input/output line
31	PIO8	I/O	Programmable input/output line
32	PIO9	I/O	Programmable input/output line
33	PIO10	I/O	Programmable input/output line
34	PIO11	I/O	Programmable input/output line

Support A-law, μ-law and CVSD digitize audio CODEC in PCM interface

6. Electrical Specifications

6.1 Input/Output Terminal Characteristics

Digital Terminals	Min	Typ	Max	Unit
Input Voltage Levels				
VIL input logic level low 2.7V ≤ Vcc ≤ 3.0V	-0.4	-	+0.8	V
VIH input logic level high	0.7Vcc	-	Vcc+0.4	V
Output Voltage Levels				

VOL output logic level low (Io = 4.0mA), 2.7V ≤ Vcc ≤ 3.0V	-	-	0.2	V
VOH output logic level high (Io = -4.0mA), 2.7V ≤ Vcc ≤ 3.0V	Vcc-0.2	-	-	V
Input and Tri-state Current with				
Strong pull-up	-100	-40	-10	μA
Strong pull-down	+10	+40	+100	μA
Weak pull-up	-5.0	-1.0	-0.2	μA
Weak pull-down	+0.2	+1.0	+5.0	μA
I/O pad leakage current	-1	0	+1	μA
CI Input Capacitance	1.0	-	5.0	pF
USB Terminals	Min	Typ	Max	Unit
Vcc for correct USB operation (1)	3.1	-	3.6	V
Input threshold				
VIL input logic level low	-	-	0.3Vcc	V
VIH input logic level high	0.7Vcc	-	-	V
Input leakage current				
0V < VIN < Vcc(1)	-1	1	5	μA
CI Input capacitance	2. 5	-	10.0	pF
Output Voltage levels To correctly terminated USB Cable				
VOL output logic level low	0.0	-	0.2	V
VOH output logic level high	2.8	-	Vcc	V

Notes:

(1) while using USB,Vcc>3.1V.

6.2 Auxilliary ADC

Auxiliary ADC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Input voltage range (LSB size = Vref/255)	0	-	Vref	V
Accuracy INL(Guaranteed monotonic)	-1	-	1	LSB
Accuracy DNL (Guaranteed monotonic)	0	-	1	LSB
Offset	-1	-	1	LSB
Gain Error	-0.8	-	0.8	%
Input Bandwidth	-	100	-	kHz
Conversion time	-	2.5	-	μs
Sample rate(a)	-	-	700	Samples/s

6.3 Absolute Maximum ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the Module are listed below; exceeding these values will cause permanent damage.

Parameter	Min	Max	Unit
Peak current of power supply	0	75	mA

Voltage at digital pins	-0.3	3.6	V
Voltage at POWER pin	2.7	3.6	V

6.4 Power Consumption

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Page scan	-	115.2	0.42	mA
Inquiry and page scan	-	115.2	0.76	mA
ACL No traffic	Master	115.2	4.60	mA
ACL With file transfer	Master	115.2	10.3	mA
ACL No traffic	Slave	115.2	17.0	mA
ACL With file transfer	Slave	115.2	24.7	mA
ACL 40ms sniff	Master	38.4	2.40	mA
ACL 1.28s sniff	Master	38.4	0.37	mA
SCO HV1	Master	38.4	39.2	mA
SCO HV3	Master	38.4	20.3	mA
SCO HV3 30ms sniff	Master	38.4	19.8	mA
ACL 40ms sniff	Slave	38.4	2.11	mA
ACL 1.28s sniff	Slave	38.4	0.42	mA
Parked 1.28s beacon	Slave	38.4	0.20	mA
SCO HV1	Slave	38.4	39.1	mA
SCO HV3	Slave	38.4	24.8	mA
SCO HV3 30ms sniff	Slave	38.4	19.0	mA
Standby Host connection(a)	-	38.4	40	uA
Reset (RESETB low)(a)	-	-	34	uA

(a) Low power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode .

7. Radio Characteristics - Basic Data Rate

Important Notes

BlueCore4 meets the Bluetooth v2.1 + EDR specification when used in a suitable application circuit between -40° C and +105° C.

Tx output is guaranteed to be unconditionally stable over the guaranteed temperature range.

7.1 Transmitter

Radio Characteristics Vcc = 3.3V Temperature = +20° C

	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[1][2]	-	2.5	-	-6 to +4[3]	dBm
Variation in RF power over temperature range with compensation enabled (±)[4]	-	1.5	-	-	dB
Variation in RF power over temperature range with	-	2	-	-	dB

compensation disabled (±)[4]					
RF power control range	-	35	-	≥16	dB
RF power range control resolution [5]	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power F=F0 ±2MHz[6][7]	-	-40	-	≤-20	dBm
Adjacent channel transmit power F=F0 ±3MHz[6][7]	-	-45	-	≤-40	dBm
Adjacent channel transmit power F=F0>±3MHz[6][7]	-	-50	-	≤-40	dBm
Δf1avg .Maximum Modulation.	-	165	-	140< Δf1avg <175	kHz
Δf2max .Minimum Modulation.	-	150	-	≥115	kHz
Δf2avg / Δf1avg	-	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz /50μS
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz
2nd Harmonic content	-	-65	-	≤-30	dBm
3rd Harmonic content	-	-45	-	≤-30	dBm

Notes:

(1) BlueCore4 firmware maintains the transmit power to be within the Bluetooth v2.1 + EDR specification limits.

(2) Measurement made using a PSKEY_LC_MAX_TX_POWER setting corresponds to a PSKEY_LC_POWER_TABLE power table entry of 63.

(3) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification.

(4) To some extent these parameters are dependent on the matching circuit used, and its behaviour over temperature. Therefore these parameters may be beyond CSR's direct control.

(5) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level >20.

(6) Measured at F0= 2441MHz.

(7) Up to three exceptions are allowed in the Bluetooth v2.1 + EDR specification. BlueCore4 is guaranteed to meet the ACP performance as specified by the Bluetooth v2.1 + EDR specification.

Radio Characteristics Vcc = 3.3V Temperature = +20° C (Continued)

Emitted power in cellular bands measured at the unbalanced port of the balun. Output power ≤4dBm. Unit = dBm/Hz

Frequency (GHz)	Min	Typ	Max	Cellular Band
0.869 - 0.894[1]	-	≤-145	-	GSM 850
0.869 - 0.894[2]	-	≤-145	-	CDMA 850
0.925 - 0.960[1]	-	≤-145	-	GSM 900
1.570 - 1.580[3]	-	≤-145	-	GPS

1.805 - 1.880[1]	-	≤-145	-	GSM 1800 / DCS 1800
1.930 - 1.990[4]	-	≤-145	-	PCS 1900
1.930 - 1.990[1]	-	≤-145	-	GSM 1900
1.930 - 1.990[2]	-	≤-145	-	CDMA 1900
2.110 - 2.170[2]	-	≤-142	-	W-CDMA 2000
2.110 - 2.170[5]	-	≤-144	-	W-CDMA 2000

Notes:

(1) Integrated in 200kHz bandwidth and then normalised to a 1Hz bandwidth.

(2) Integrated in 1.2MHz bandwidth and then normalised to a 1Hz bandwidth.

(3) Integrated in 1MHz bandwidth. and then normalised to a 1Hz bandwidth

(4) Integrated in 30kHz bandwidth and then normalised to a 1Hz bandwidth.

(5) Integrated in 5MHz bandwidth and then normalised to a 1Hz bandwidth.

7.2 Receiver

Radio Characteristics Vcc = 3.3V Temperature = +20° C

	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-84	-	≤-70	dBm
	2.441	-	-84	-		
	2.480	-	-85	-		
Maximum received signal at 0.1% BER		-	10	-	≤-20	dBm
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Continuous power required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30 - 2000	-	TBD	-	≤-10	dBm
	2000 - 2400	-	TBD	-	≤-27	
	2500 - 3000	-	TBD	-	≤-27	
	3000 - 3300	-	TBD	-	≤-10	
C/I co-channel		-	6	-	≤11	dB
Adjacent channel selectivity C/I F=F0 +1MHz[1] [2]		-	-5	-	≤0	dB
Adjacent channel selectivity C/I F=F0 -1MHz[1] [2]		-	-4	-	≤0	dB
Adjacent channel selectivity C/I F=F0 +2MHz[1] [2]		-	-38	-	≤-30	dB
Adjacent channel selectivity C/I F=F0 -2MHz[1] [2]		-	-23	-	≤-20	dB
Adjacent channel selectivity C/I F≥F0 +3MHz[1] [2]		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I F≤F0 -5MHz[1] [2]		-	-44	-	≤-40	dB
Adjacent channel selectivity C/I F=FImage[1] [2]		-	-22	-	≤-9	dB
Maximum level of intermodulation interferers [3]		-	-30	-	≥-39	dBm
Spurious output level [4]		-	TBD	-	-	dBm/Hz

Notes:

(1) Up to five exceptions are allowed in the Bluetooth v2.1 + EDR specification. BlueCore4 is guaranteed to meet the C/I performance as specified by the Bluetooth v2.1 + EDR specification.

(2) Measured at F0 = 2441MHz

(3) Measured at f1-f2 = 5MHz. Measurement is performed in accordance with Bluetooth

RF test RCV/CA/05/c. i.e. wanted signal at -64dBm

(4) Measured at the unbalanced port of the balun. Integrated in 100kHz bandwidth and then normalized to 1Hz. Actual figure is typically below TBD dBm/Hz except for peaks of -52dBm inband at 2.4GHz and ≤80dBm at 3.2GHz

8. UART Interface

BlueCore4-External Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard(1).

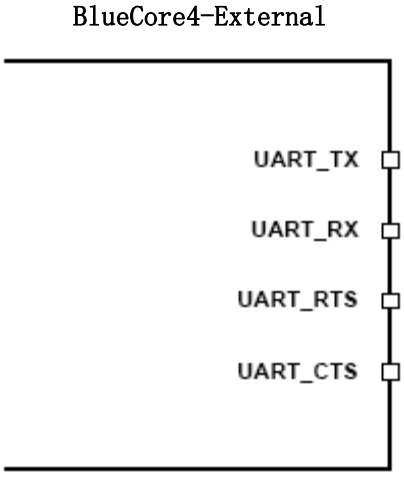


Figure 11.12: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 11.12. When BlueCore4-External is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and Vcc.

UART configuration parameters, such as Baud rate and packet format, are set using BlueCore4-External software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

(1) Uses RS232 protocol but voltage levels are 0V to VDD_USB, (requires external RS232 transceiver chip)

Parameter		Possible Values
Baud Rate	Minimum	1200 Baud (≤2%Error)
		9600 Baud (≤1%Error)
	Maximum	3.0MBaud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2

Bits per channel	8

Table 11.7: Possible UART Settings

The UART interface is capable of resetting BlueCore4-External upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 11.13. If tBRK is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur.

This feature allows a host to initialise the system to a known state. Also, BlueCore4-External can emit a Break character that may be used to wake the Host.

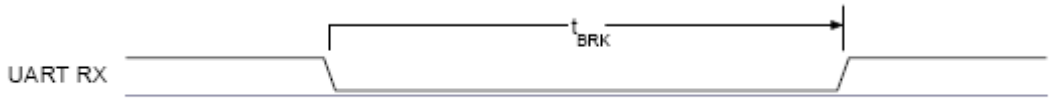


Figure 11.13: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used.This initial flash programming can be done via the SPI.

Table 11.3 shows a list of commonly used Baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the Persistent Store Key according to the formula in Equation 11.7.

$$\text{Baud Rate} = \text{PSKEY\_UART\_BAUD\_RATE} / 0.004096$$

Equation 11.7: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 11.8: Standard Baud Rates

8.1 UART Bypass

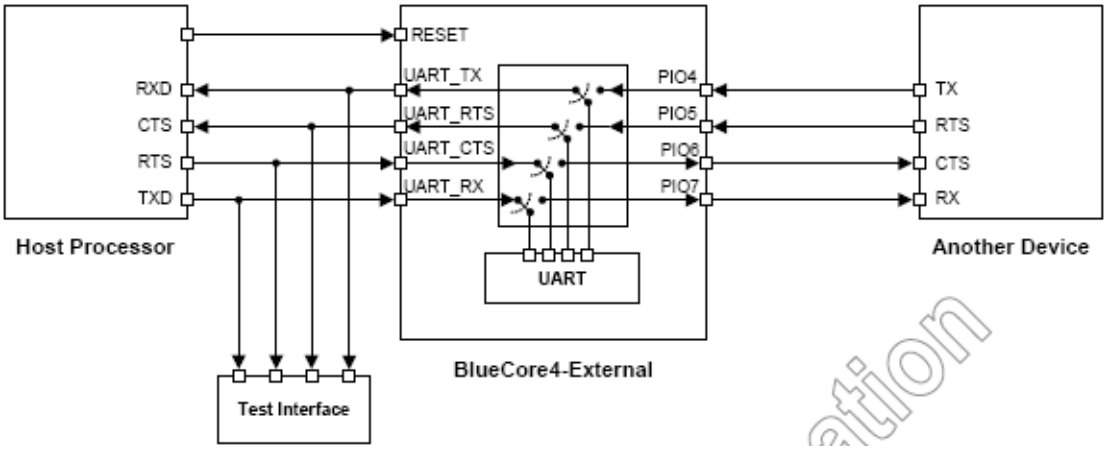


Figure 11.14: UART Bypass Architecture

8.2 UART Configuration While RESET is Active

The UART interface for BlueCore4-External while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore4-External reset is de-asserted and the firmware begins to run.

8.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore4-External can be used. The default state of BlueCore4-External after reset is de-asserted, this is for the host UART bus to be connected to the BlueCore4-External UART, thereby allowing communication to BlueCore4-External via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore4-External upon this, it will switch the bypass to PIO[7:4] as shown in Figure 11.14. Once the bypass mode has been invoked, BlueCore4-External will enter the deep sleep state indefinitely.

In order to re-establish communication with BlueCore4-External, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

8.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

9. USB Interface

BlueCore4-External USB devices contain a full speed (12Mbits/s) USB interface

that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth v2.1 + EDR specification or alternatively can appear as a set of endpoint appropriate to USB audio devices such as speakers.

As USB is a Master/Slave oriented system (in common with other USB peripherals), BlueCore4-External only supports USB Slave operation.

9.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4-External and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP / USB_DN and the cable.

9.2 USB Pull-Up Resistor

BlueCore4-External features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4-External is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

9.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V.

CSR recommends 3.3V for optimal USB signal quality.

9.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore4-External via a resistor network (Rvb1 and Rvb2), so BlueCore4-External can detect when VBUS is powered up. BlueCore4-External will not pull USB_DP high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO

line is allocated for USB pull-up purposes. A 1.5K 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in BlueCore is only suitable for bus powered USB devices i.e. dongles.

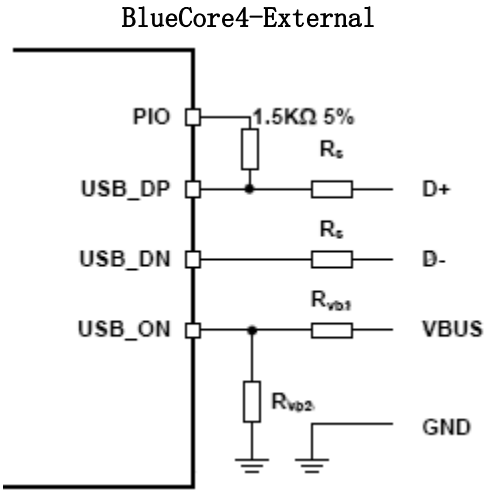


Figure 11.15: USB Connections for Self Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Note:

USB_ON is shared with BlueCore4-External PIO terminals

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 11.9: USB Interface Component Values

9.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable.BlueCore4-External negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus powered mode, BlueCore4-External requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than

10μF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore4-External will result in reduced receive sensitivity and a distorted RF transmit signal.

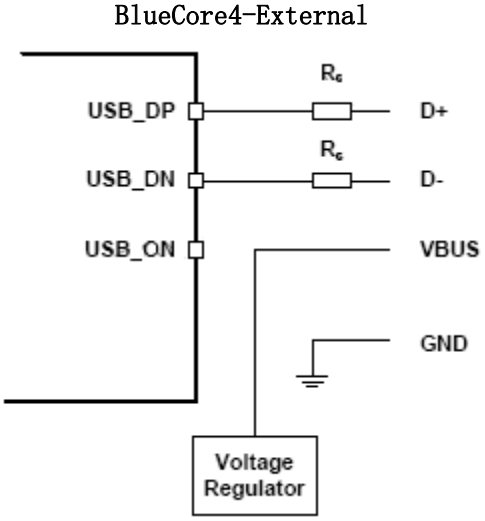


Figure 11.16: USB Connections for Bus Powered Mode

9.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB Suspend mode. While in USB Suspend,bus powered devices must not draw more than 0.5mA from USB VBUS (self powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore4-External.

The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see separate CSR documentation).

9.7 Detach and Wake-Up Signalling

BlueCore4-External can provide out-of-band signalling to a host controller by using the control lines called “USB_DETACH” and “USB_WAKE_UP”. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4-External into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore4-External to put USB_DN and USB_DP in a high impedance state and turned off the pull-up resistor

on D+. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4-External will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while BlueCore4-External is effectively disconnected from the bus.

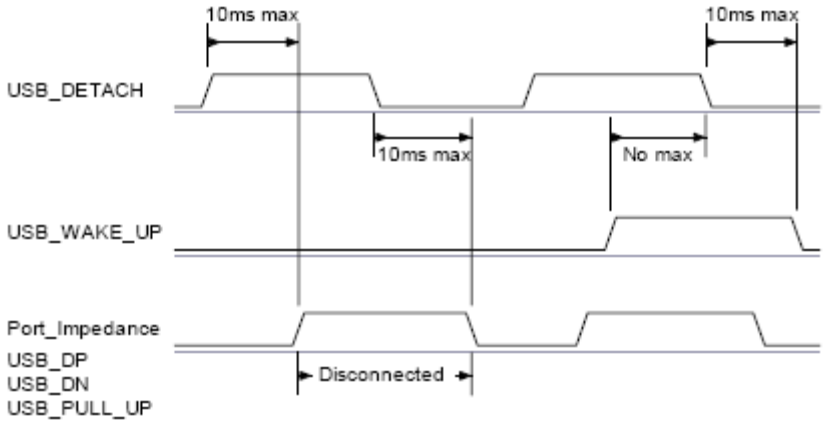


Figure 11.17: USB_DETACH and USB_WAKE_UP Signal

9.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4-External and Bluetooth software running on the host computer. Suitable drivers are available from www.csrsupport.com.

9.9 USB 1.1 Compliance

BlueCore4-External is qualified to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore4-External meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

9.10 USB 2.0 Compatibility

BlueCore4-External is compatible with USB v2.0 host controllers; under these

circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

10. PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, BlueCore4-External has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore4-External offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-External allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time(1).

BlueCore4-External can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz.When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore4-External is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

BlueCore4-External interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-External is also compatible with the Motorola SSI™ interface

Note:

(1) Subject to firmware support, contact CSR for current status.

10.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore4-External generates PCM_CLK and PCM_SYNC.

BlueCore4-External

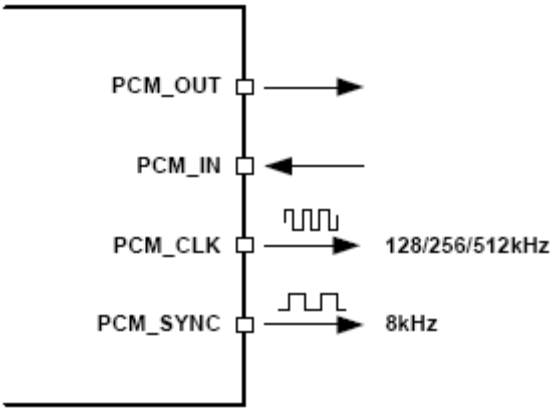


Figure 11.20: BlueCore4-External as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore4-External accepts PCM_CLK rates up to 2048kHz.

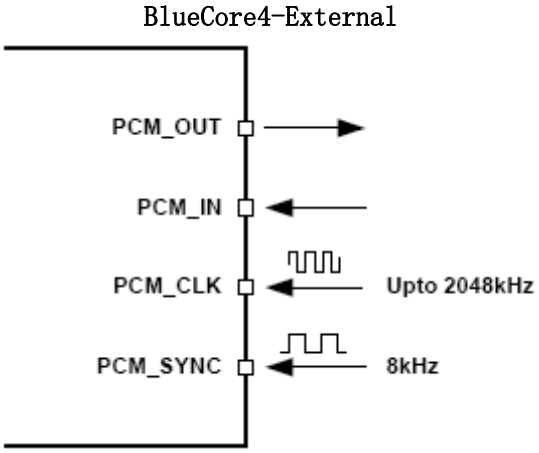


Figure 11.21: BlueCore4-External as PCM Interface Slave

10.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-External is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-External is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5μs long.

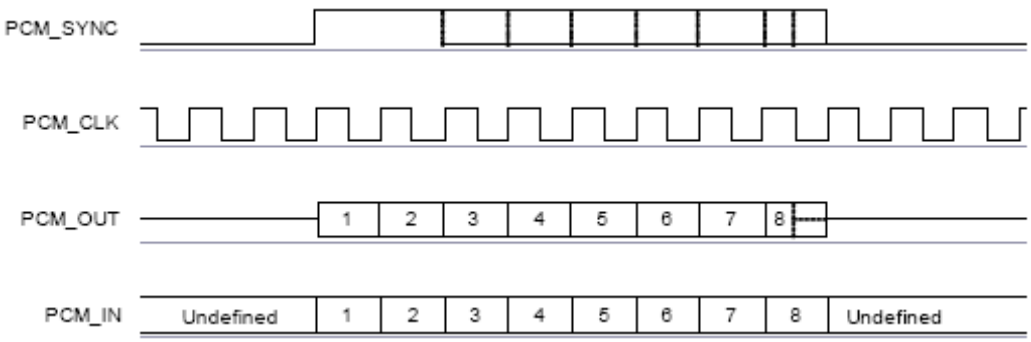


Figure 11.22: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-External samples PCM_IN on the falling edge of PCM_CLK and transmits

PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

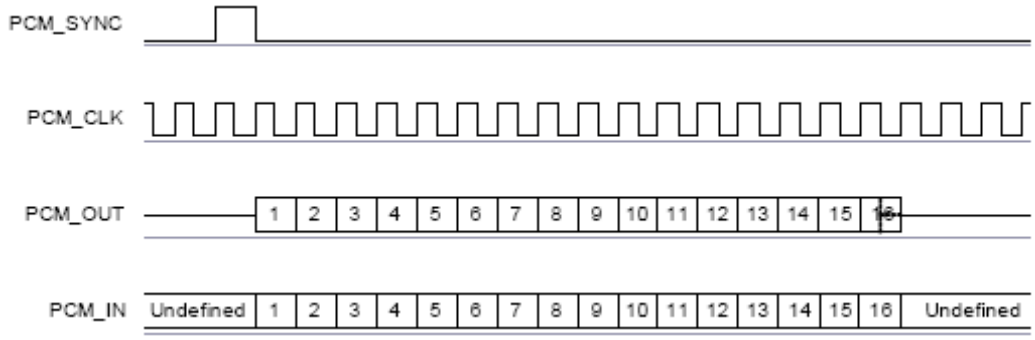


Figure 11.23: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.4 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

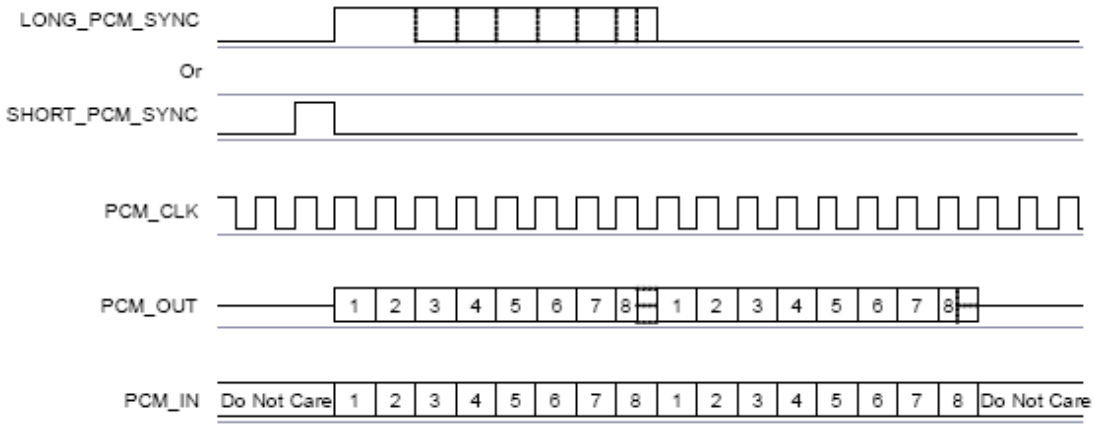


Figure 11.24: Multi Slot Operation with Two Slots and 8-bit Companded Samples

10.5 GCI Interface

BlueCore4-External is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

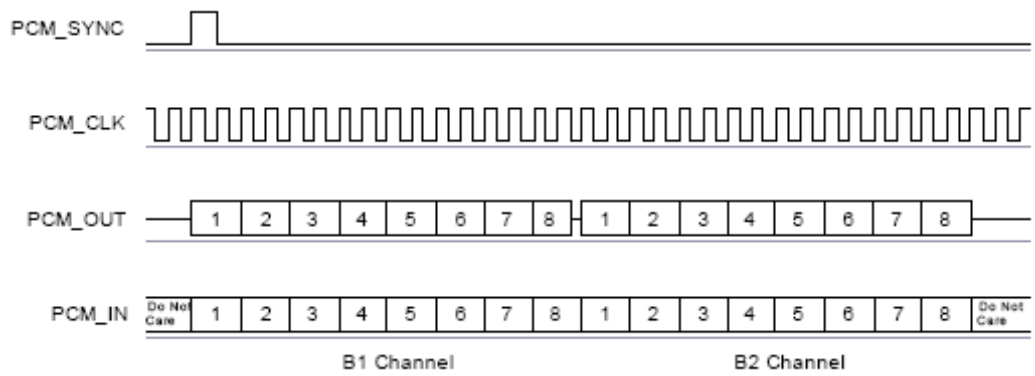


Figure 11.25: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4-External in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

10.6 Slots and Sample Formats

BlueCore4-External can receive and transmit on any selection of the first four slots following each sync pulse.Slot durations can be either 8 or 16 clock cycles. Duration's of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

BlueCore4-External supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big Endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

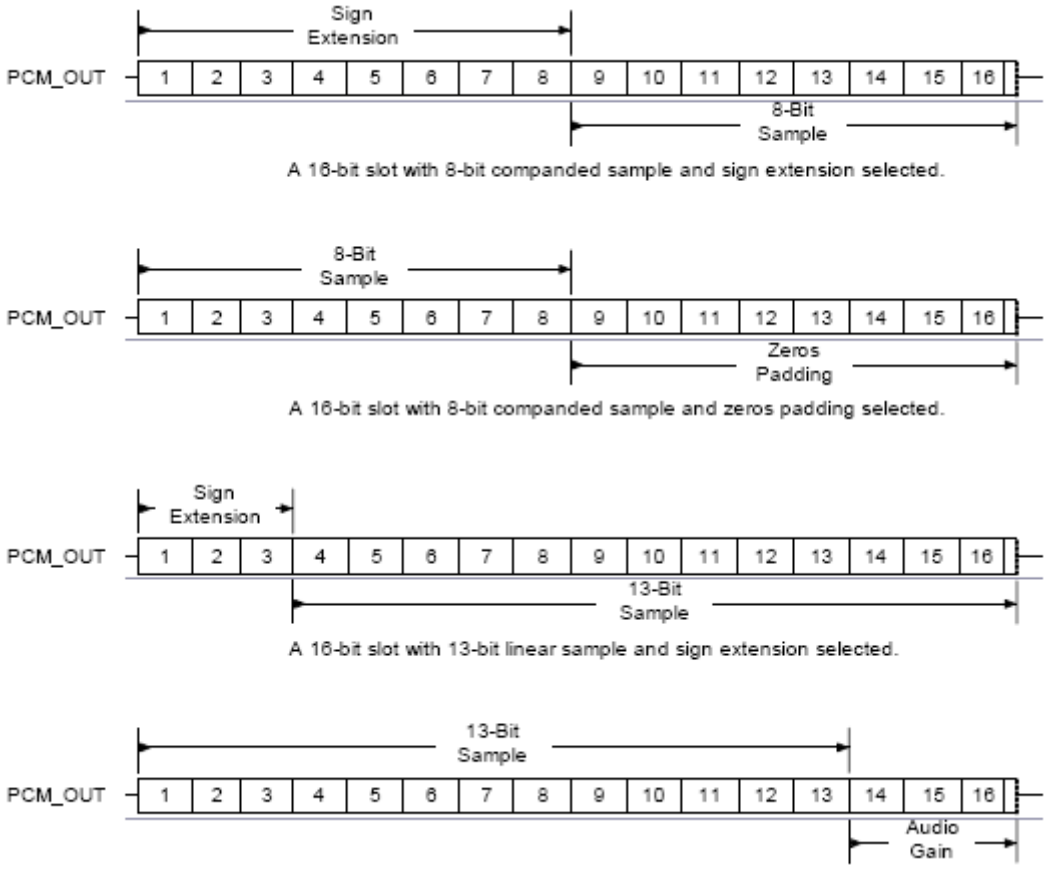


Figure 11.26: 16-Bit Slot Length and Sample Formats

10.7 Additional Features

BlueCore4-External has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

10.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 8.13.	-	128	-	kHz
			-	256	-	
			-	512	-	
		48MHz DDS generation. Selection of frequency is programmable. See Table 8.14 and PCM_CLK and PCM_SYNC Generation.	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh} (a)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (a)	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk

$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)	-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance	-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low	30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	10	-	-	ns

Table 11.11: PCM Master Timing

Note:

(1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

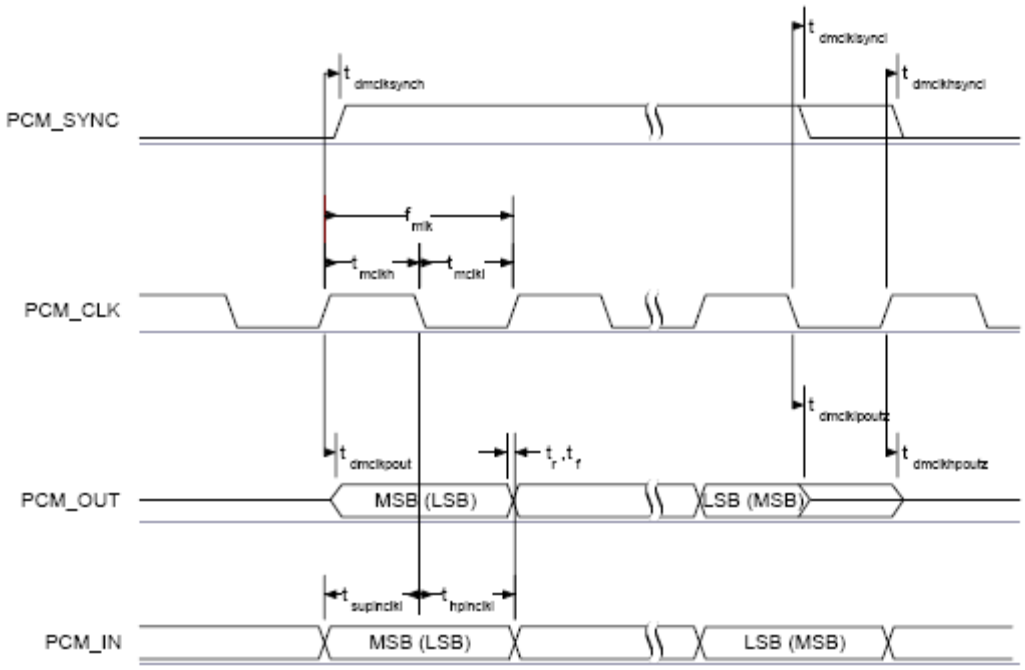


Figure 11.27: PCM Master Timing Long Frame Sync

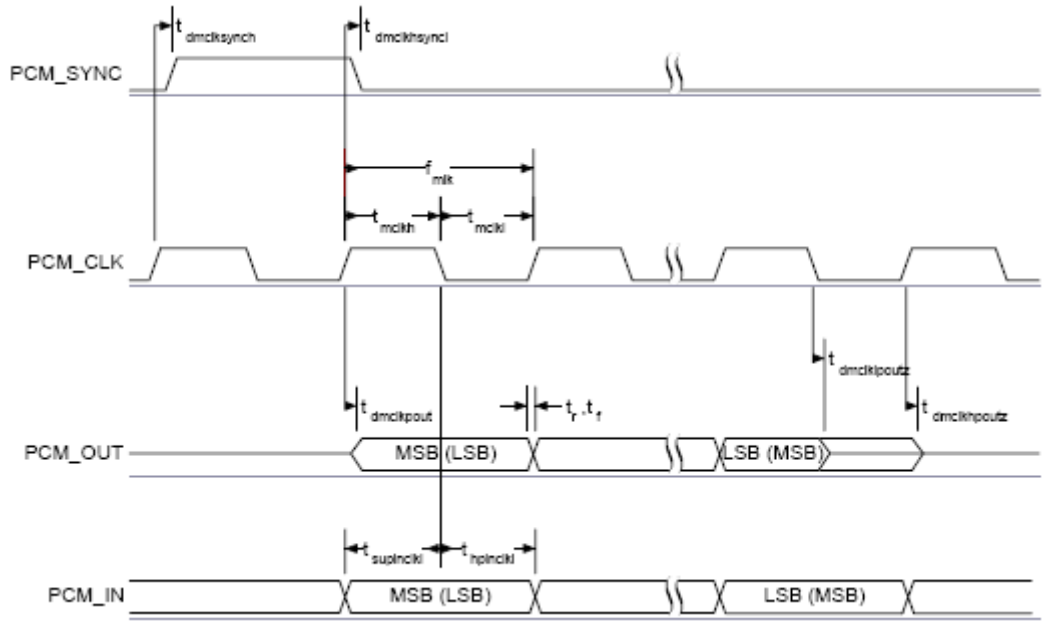


Figure 11.28: PCM Master Timing Short Frame Sync

10.9 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low,whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 11.12: PCM Slave Timing

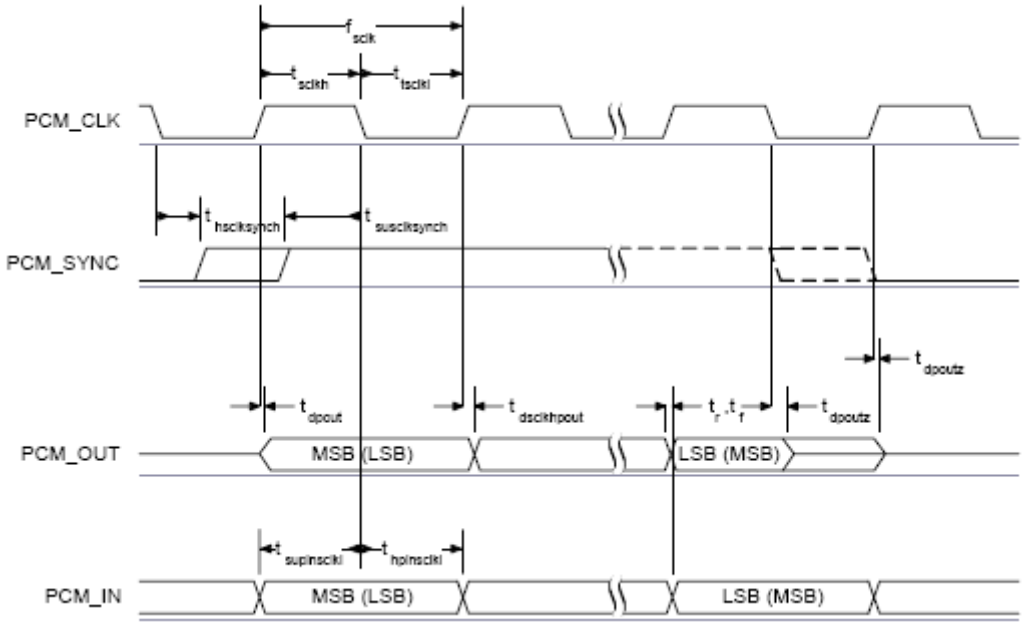


Figure 11.29: PCM Slave Timing Long Frame Sync

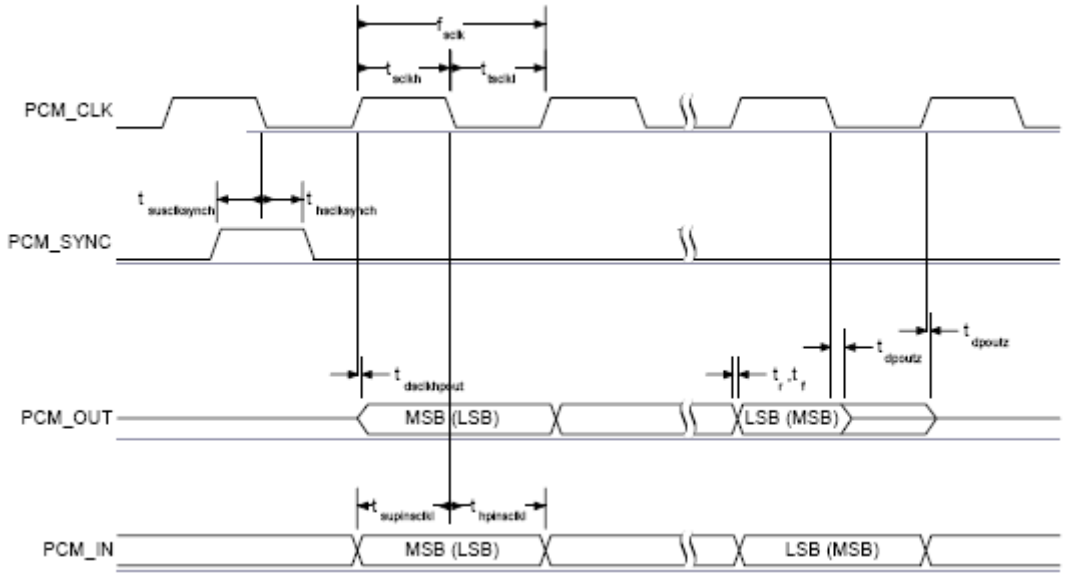


Figure 11.30: PCM Slave Timing Short Frame Sync

10.10 PCM_CLK and PCM_SYNC Generation

BlueCore4-External has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore4-External internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock which allows a greater range of frequencies to be generated with low jitter but consumes more power. This second method is selected by setting bit “48M_PCM_CLK_GEN_EN” in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by “LONG_LENGTH_SYNC_EN” in PSKEY_PCM_CONFIG32.

The Equation 11.8 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = CNT\_RATE / CNT\_LIMIT \times 24MHz$$

Equation 11.8: PCM_CLK Frequency When Being Generated Using the Internal 48MHz clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using following equation:

$$f = PCM\_CLK / (SYNC\_LIMIT \times 8)$$

Equation 11.9: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

10.11 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables detail these PS Keys. PSKEY_PCM_CONFIG32. The default for this key is 0x00800000 i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-stating of PCM_OUT. PSKEY_PCM_LOW_JITTER_CONFIG is described in Table 11.14.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16- bit slot by inserting extra LSBs, 1 selects sign extension.When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.

TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore4-External. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is '0001'. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 11.13: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit.
CNT_RATE	[23:16]	Sets PCM_CLK count rate.
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 11.14: PSKEY_PCM_LOW_JITTER_CONFIG Description

11. I/O Parallel Ports

Fifteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from Vcc. PIO[7:4] are powered from Vcc. AIO [2:0] are powered from Vref.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO [2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore4-External is provided from a system application specific integrated circuit (ASIC).

BlueCore4-External has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the other three may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by Vref (1.8V).

Important Note:

CSR cannot guarantee that terminal functions PIOs remain the same. Please refer to the software release note for the implementation of these PIO lines, as they are firmware build specific.

12. IIC Interface

PIO[8:6] can be used to form a Master I2C interface. The interface is formed using software to drive these lines.Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD),keyboard scanner or EEPROM.

Note:

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM cannot support UART bypass mode PIO lines need to be pulled-up through 2.2kΩ resistors.

For connection to EEPROMs, refer to CSR documentation on I2C EEPROMS for use with BlueCore. This provides information on the type of devices which are currently supported.

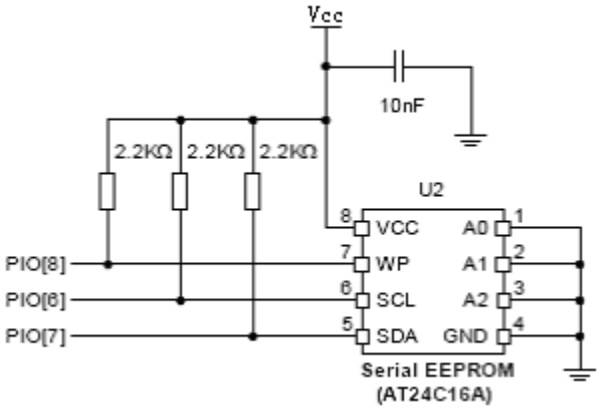


Figure 11.31: Example EEPROM Connection

13. RESETB

BlueCore4-External may be reset from several sources: RESETB pin, power on reset, a UART break character or via a software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-stated. The PIOs have weak pull-downs.

Following a reset, BlueCore4-External assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-External is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-External free runs, again at a safe frequency.

13.1 Pin States on Reset

Table 11.15 shows the pin states of BlueCore4-External on reset.

Pin Name	State: BlueCore4-External
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-stated with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-stated with weak pull-down
AIO[2:0]	Output, driving low
RESET	Input with weak pull-down
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
RF_A	High impedance
RF_B	High impedance
RX_IN	High impedance

XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 11.15: Pin States of BlueCore4-External on Reset

13.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset(1): Baud rate and RAM data not available

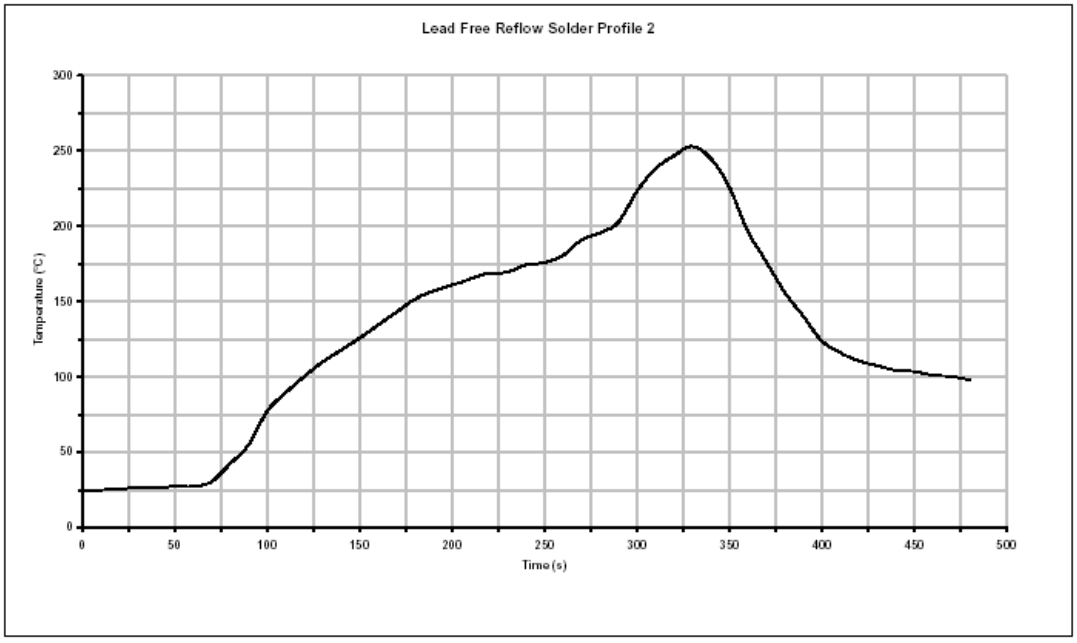
Note:

(1) Cold Reset constitutes one of the following:

- Power cycle
- System reset (firmware fault code)
- Reset signal, see Section “RESETB”

14. Solder Profiles

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%



Typical Lead-Free Re-flow Solder Profile

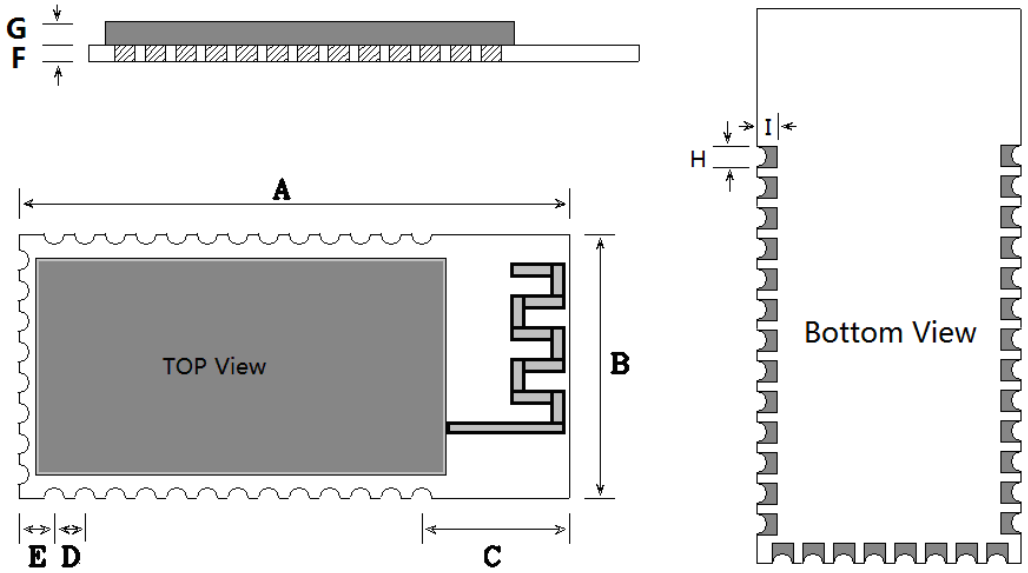
Key features of the profile:

- Initial Ramp = 1-2.5° C/sec to 175° C±25° C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250° C) = 3° C/sec max.
- Time above liquidus temperature (217° C): 45-90 seconds
- Device absolute maximum reflow temperature: 260° C

Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260° C.

Notes：They need to be baked prior to mounting。

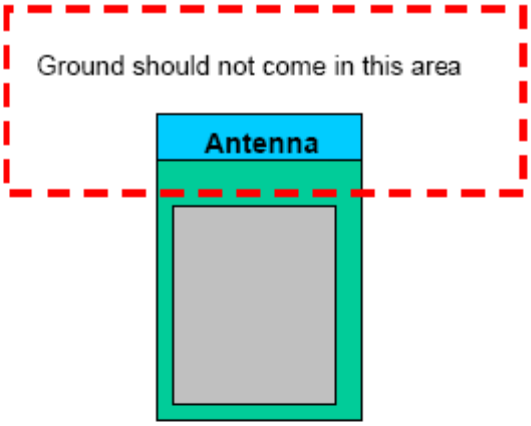
15. Physical Dimensions

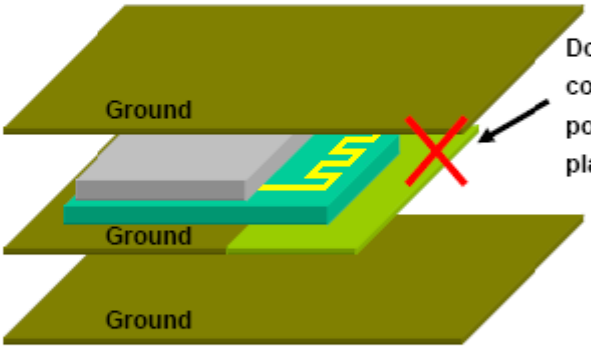


A	B	C	D	E	F	G	H	I	Unit
1063	511.8	285.4	59.1	68.9	31.5	55.1	20	32	mil
27	13	7.25	1.5	1.75	0.8	1.4	1.0	0.8	mm

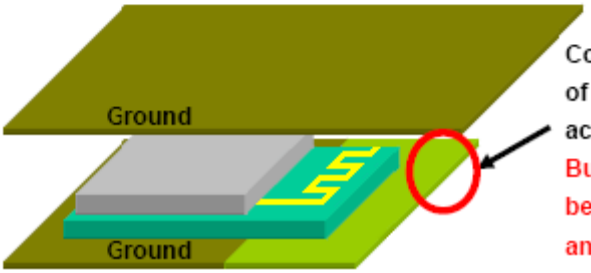
16. Guide for Antenna Radiation

In order to achieve longest communication range, please keep the area surrounding antenna free of grounding or metal housing.





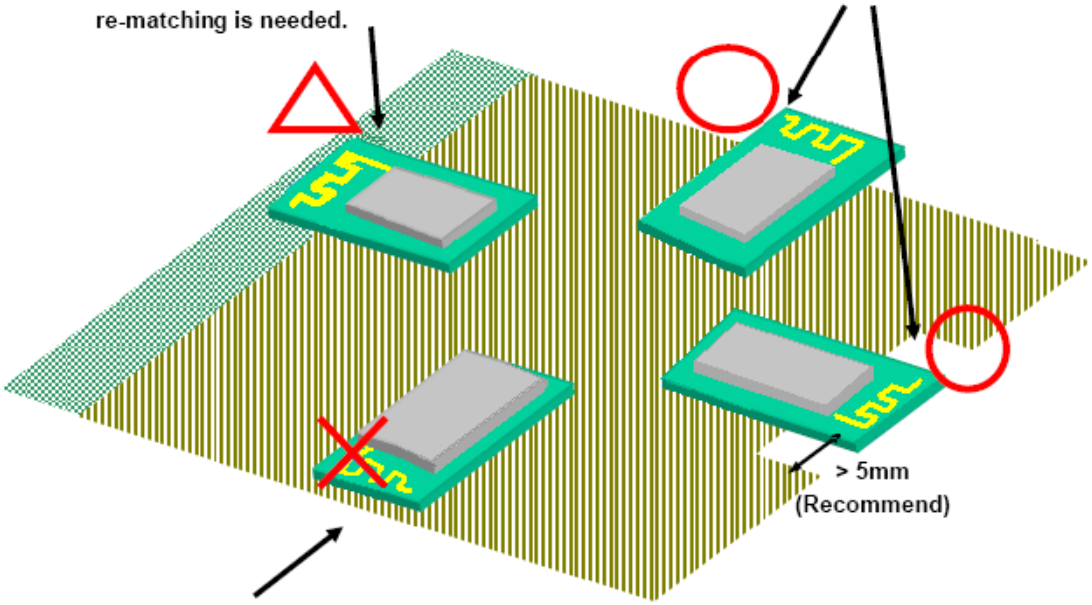
Do not completely cover the antenna portion with ground plates.



Covering only one side of the antenna is acceptable.
But the distance between ground plate and antenna should be keep as far as

If there is PCB or other material under the antenna area, antenna will be de-tuned from its resonant frequency. Impedance re-matching is needed.

When mounting on a PCB, locate it at (or near) the edge of the PCB



If mounted at an inner portion of the PCB grounded, no sufficient antenna performance will be available.

PCB with Ground Plane

PCB without Ground Plane

17. Contact information

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